Lecture 2 – Switched-Mode Power Supplies

The linear regulator. Switched-mode power supplies. Pulse-width modulation. Step-Down (buck) regulator. Step-Up (boost) regulator. Inverting regulator. Single-ended primary-inductor converter (SEPIC). Selection of components. Output filters.

Introduction

Virtually every piece of electronic equipment, e.g., computers and their peripherals, TVs and audio equipment, smart phones, industrial controllers, etc., is powered from a DC power source, be it a battery or a DC power supply. Most of this equipment requires not only DC voltage but voltage that is also well filtered and regulated. Since power supplies are so widely used in electronic equipment, these devices now comprise a large worldwide segment of the electronics market.

There are four types of electronic power conversion devices in use today which are classified as follows according to their input and output voltages:

1. AC / AC transformer
2. DC / DC converter
3. AC / DC power supply
4. DC / AC inverter

DC power is usually available to a digital system in the form of a system power supply or battery. This power may be in the form of 5 V, 12 V, 28V, 48V or other DC voltages. Since voltages are low, isolation is not usually required. We will therefore look closely at DC / DC converters used in digital electronics.

2.2

A power supply converting AC line voltage to DC power must perform the following functions at high efficiency and at low cost:

1. Rectification: Convert the incoming AC line voltage to DC voltage.
2. Voltage transformation: Supply the correct DC voltage level(s).
3. Filtering: Smooth the ripple of the rectified voltage.
4. Regulation: Control the output voltage level to a constant value irrespective of line, load and temperature changes.
5. Isolation: Separate electrically the output from the input voltage source.
6. Protection: Prevent damaging voltage surges from reaching the output; provide back-up power or shut down during a brown-out.

An ideal power supply would be characterized by supplying a smooth and constant output voltage regardless of variations in the voltage, load current or ambient temperature at 100% conversion efficiency. The figure below compares a real power supply to this ideal one and further illustrates some power supply terms:

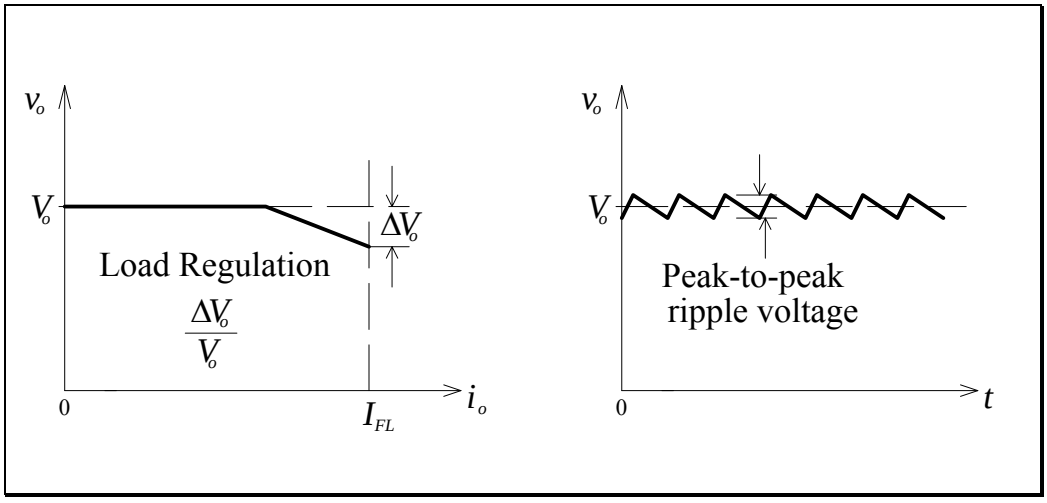
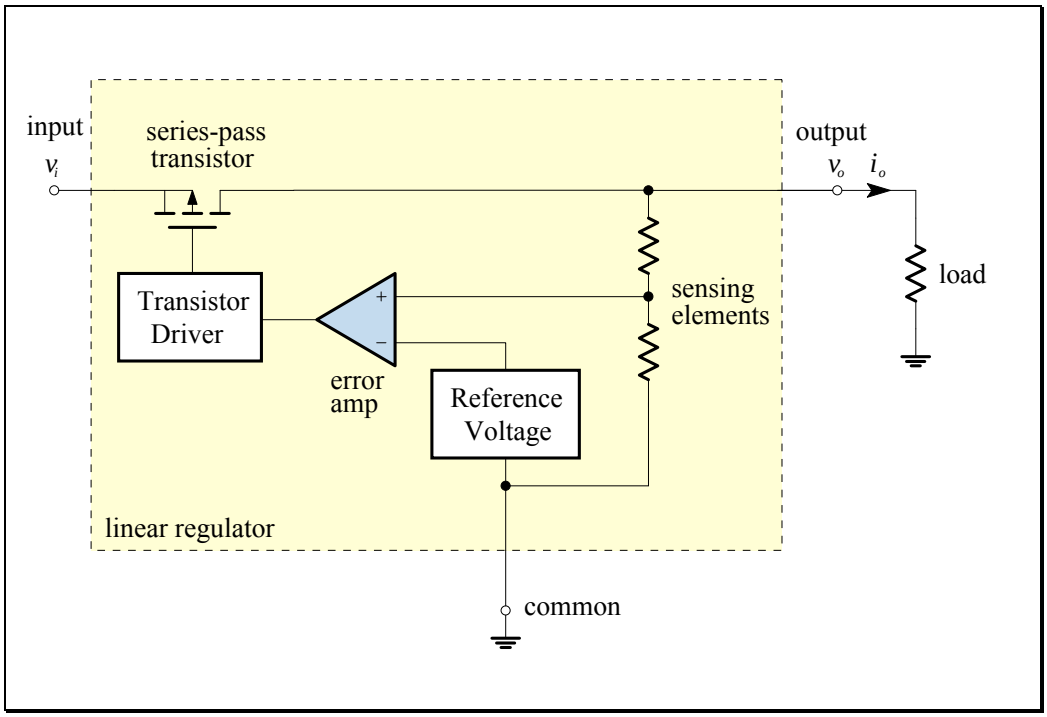


Figure 2.1 – A real power supply has error compared to an ideal supply

The Linear Regulator

The basic topology for a linear regulator is shown below:



The basic topology of a linear regulator

Figure 2.2 – The basic topology of a linear regulator

It consists of a transistor, operating in the linear region, that acts as a variable resistance between the DC input and the DC output terminals. The error amplifier senses the DC output voltage, compares it with a voltage reference, and creates an error signal which then drives the gate (or base) of the transistor via a drive circuit. If the DC output voltage increases (say, as a result of either an increase in input voltage or a decrease in output load current), the drive to the *series-pass* transistor is reduced. This increases the resistance of the series-pass element and hence controls the output voltage so that the sampled output continues to track the reference voltage. This negative-feedback loop works in the reverse direction for any decreases in output voltage, thus maintaining the DC output voltage at a constant value.

Linear regulators are relatively low cost, have a low component count, and offer excellent performance and high reliability.

2.4

In general, any difference between the input voltage and the constant output voltage is "dropped" across the transistor. Thus, the linear regulator is not very efficient, since the series-pass element must dissipate a power given by:

The power dissipated by the series-pass transistor

$$P = (v_i - V_o) i_o \tag{2.1}$$

For example, if a 9 V battery is used to obtain a 5 V supply, then the efficiency of a power supply using a linear regulator is:

$$\begin{aligned} \eta &= \frac{\text{output power}}{\text{input power}} \times 100\% \qquad (2.2) \\ &\approx \frac{V_o I_o}{V_i I_o} \times 100\% \\ &= \frac{V_o}{V_i} \times 100\% \\ &= \frac{5}{9} \times 100\% \\ &= 55.56\% \end{aligned}$$

Linear regulators are not particularly efficient…

This is not efficient compared to switching regulators, which can achieve efficiencies up to 95%. The power lost in the voltage conversion is dissipated as heat in the regulator, and for this reason linear regulators may need to be fitted with a heat sink.

…but they do not generate RFI noise

There is no switching action within the linear regulator control loop, and so there is no *radio frequency interference* (RFI) produced by this type of regulator. This lower RFI noise can be a major advantage in some applications, and for this reason, linear regulators still have a place in modern power supply applications even though the efficiency is quite low.

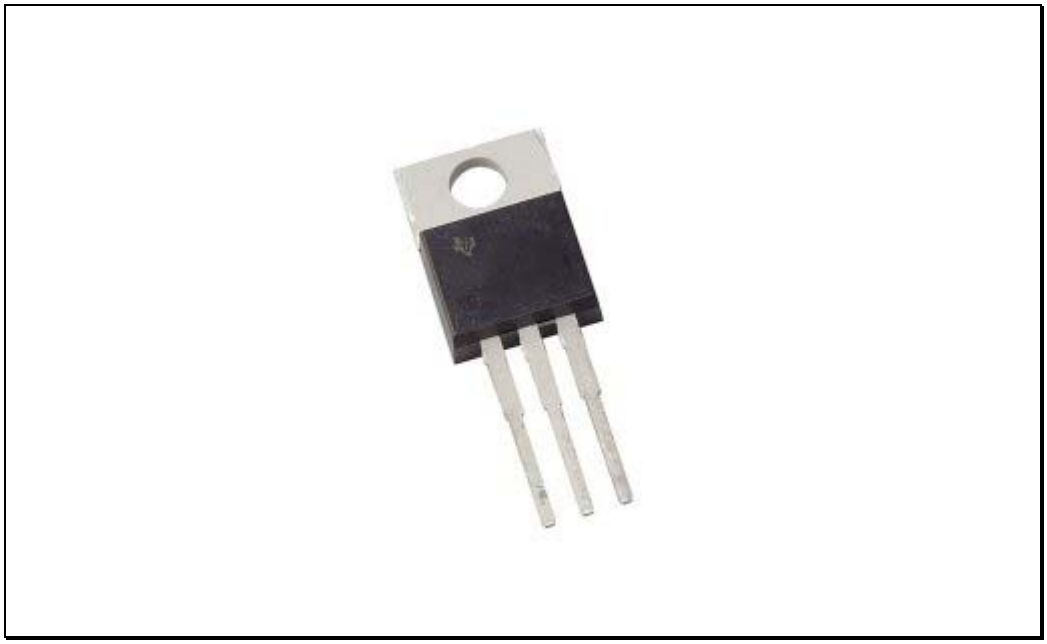
Limitations of the Linear Regulator

Linear regulators have the following limitations:

- The linear regulator is constrained to produce only a lower regulated voltage from a higher non-regulated input.
- The output always has one terminal that is common with the input. This can be a problem, complicating the design when DC isolation is required between input and output or between multiple outputs.
- The raw DC input voltage is usually derived from the rectified secondary of a 50-60 Hz transformer whose weight and volume is often a serious constraint.
- The regulation efficiency is very low, resulting in a considerable power loss needing large heat sinks in relatively large and heavy power units.

Limitations of the linear regulator

A typical package for a linear regulator is shown below, which shows a large metal tab to help dissipate heat, with a hole for securing to an external heat sink if necessary.



A typical 3-pin package for a linear regulator – the TO-220

Figure 2.3 – A typical 3-pin package for a linear regulator – the TO-220

2.6

Pulse-Width Modulation

In the early 1960's, switching regulators started to be designed for the military, who would pay a premium for light weight and efficiency. One way to control average power to a load is to control average voltage applied to it. This can be done by moving a single-pole double-throw switch between the input voltage (V_i) and common (0) in rapid fashion as being done in the figure below:

A PWM waveform used to obtain an average (DC) output voltage

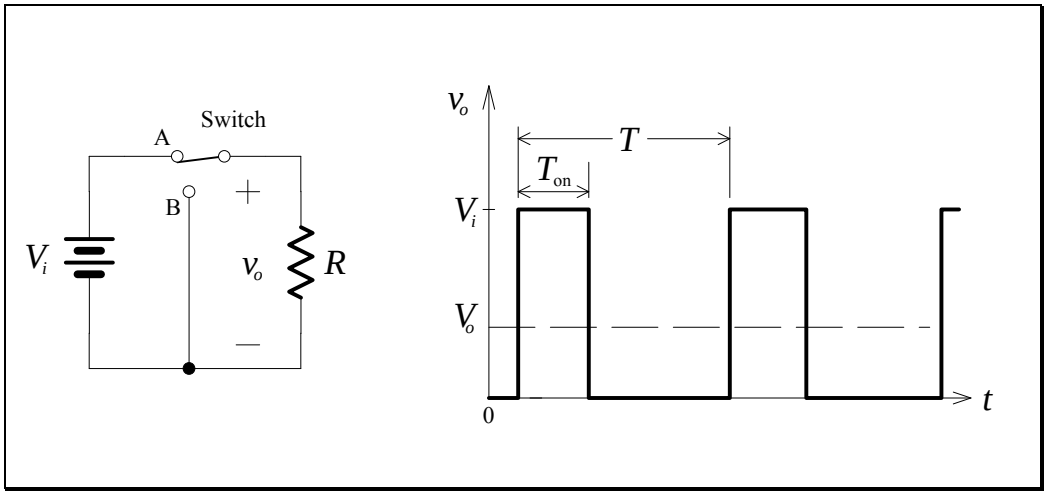


Figure 2.4 – Example of pulse width modulation

The average voltage seen by the load resistor *R* is equal to:

$$V_o = v_{o,\text{avg}} = \left(\frac{T_{\text{on}}}{T}\right)V_i = DV_i \tag{2.3}$$

The duty cycle, $D = T_{\text{on}}/T$, represents the amount of "on" time compared to the period. Varying T_{on}, and therefore the duty, *D*, varies V_o. This method of control is referred to as pulse-width modulation (PWM).

If the PWM waveform is applied to a lowpass output filter before it reaches the load, then the load effectively sees a regulated DC voltage. Usually the lowpass filter would be an inductor and an output capacitor.

There are many different switching voltage regulator designs, but all rely on a method of PWM to control the output voltage.

Switched-Mode Power Supplies

A switched-mode power supply (SMPS) operates by rapidly switching a transistor between two efficient operating states: *cutoff*, where there is a high voltage across the transistor but no current; and *saturation*, where there is a high current through the transistor but at a very small voltage drop. Essentially, the transistor operates as a power switch that creates an AC voltage from the DC input voltage. This AC voltage can be stepped up or down and then filtered back to DC.

SMPSs are popular due to their high efficiency and high power density. The table below compares some of the salient features of both linear and switched-mode power supplies.

Specification	**Linear**	**Switched-Mode**
Line Regulation	0.02%–0.05%	0.05%–0.1%
Load Regulation	0.02%–0.1%	0.1%–1.0%
Output Ripple	0.5 mV–2 mV RMS	10 mV–100 mVp-p
Input Voltage Range	±10%	±20%
Efficiency	40%–55%	60%–95%
Power Density	30 mW/cm^3	10 mW–600 mW/cm^3
Transient Recovery	50 µs	300 µs
Hold-Up Time	2 ms	34 ms

Table 2.1 - Linear vs. switched-mode power supplies (typical)

The main advantages of a switching regulator over a linear regulator are the higher efficiency and the greater flexibility offered by output voltages that are less than, greater than, or of opposite polarity to the input voltage.

The downside of a switching regulator design is that it is considerably more complex. In addition, the output voltage contains switching noise, which must be removed for many applications.

Line and load regulation are usually better with linear supplies, sometimes by as much as an order of magnitude, but switching power supplies frequently use linear postregulators to improve output regulation.

The *hold-up time* is the amount of time that a power supply can maintain output within the specified voltage range after a loss of input power. In linear power supplies the time the output fails following the failure of the input is almost immediate. In switching power supplies, energy is stored in inductors and capacitors, providing a useable hold-up time to protect against transient power outages. Hold-up time is a function of the energy storage capability of the power supply and the specific loading of the power supply.

Switching Regulator Configurations

There are three basic configurations of switching regulator:

- Step-Down, or “buck”
- Step-Up, or “boost”
- Inverting

These are shown below:

Switching regulator configurations

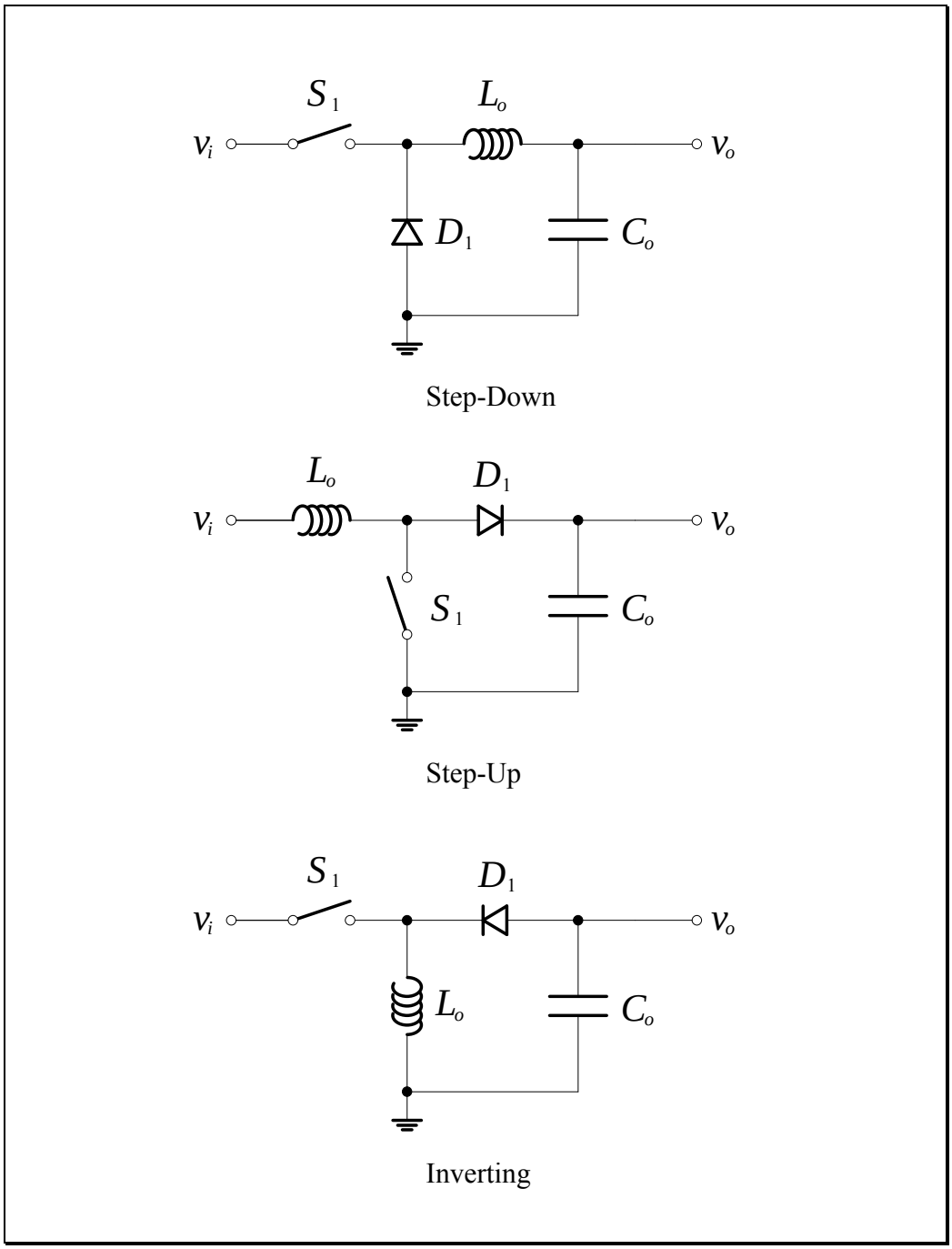


Figure 2.5 –Switching regulator configurations

2.10

Step-Down (Buck) Regulator

The circuit in Figure 2.4 can be modified by adding an *LC* filter between the switch and the load:

PWM circuit with *LC* filter

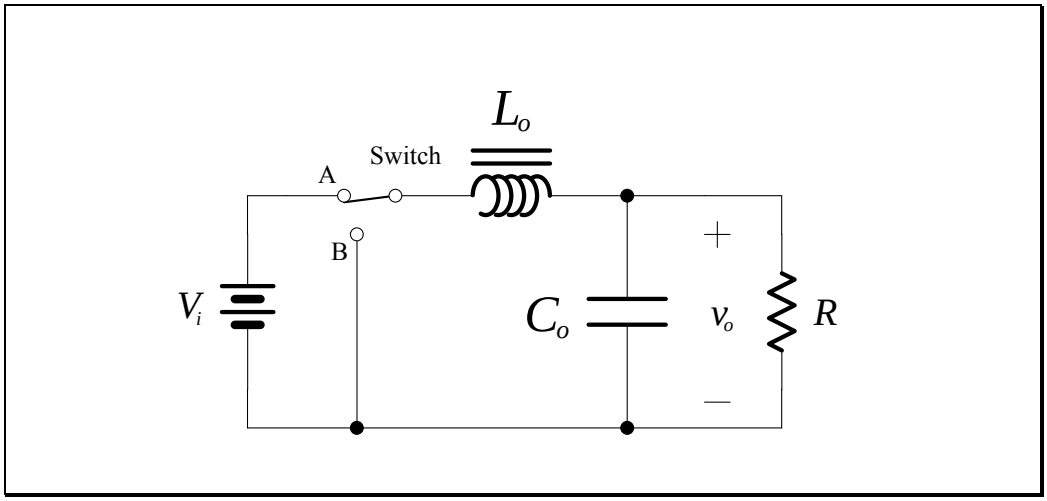


Figure 2.6 – PWM circuit with *LC* filter

When the switch is in position A, the current through the inductor increases and the energy stored in the inductor increases. When the switch is in position B, the current through the inductor decreases and the energy stored in the inductor decreases. During this period the inductor delivers some of its stored energy to the load resistor. The capacitor reduces the ripple content in the output voltage, since it presents a low impedance to high frequency alternating currents compared to the load.

The circuit in Figure 2.6 contains a single-pole double-throw switch, which is difficult to realize using power semiconductor devices. On the other hand, an understanding of the circuit leads to a realizable and simple configuration. When the switch is in position A, the current through the inductor increases and it decreases when the switch is in position B. It is possible to have a power semiconductor device such as a MOSFET acting as a switch to replace the switch in position A. When the switch is in position B, the inductor current "freewheels" through it and hence a diode can be used for freewheeling operation. Then only the MOSFET needs to be controlled, and in practice a pulse-width modulating IC is used. The circuit that results is known as a step-down regulator.

The step-down regulator, also known as a buck regulator, is shown below:

The step-down regulator circuit

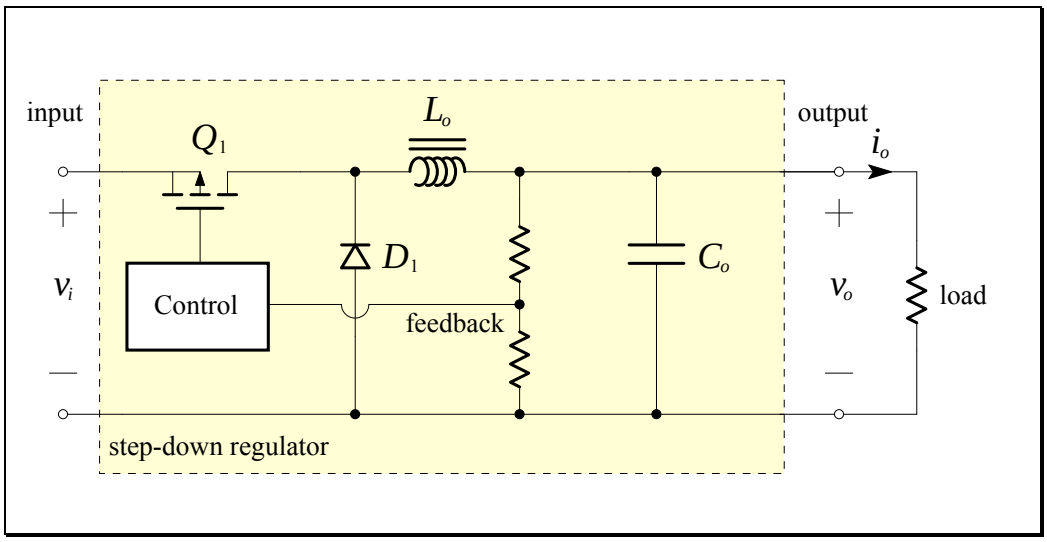


Figure 2.7 – Step-down regulator circuit

When the controller senses that the output voltage v_o is too low, the pass transistor Q_1 is turned "hard on", which applies the input voltage to the left-hand side of the inductor, and reverse biases D_1. Current builds up in L_o, storing magnetic energy, and the output capacitor C_o starts to recharge. At a predetermined level of v_o, the controller switches off the pass transistor Q_1, which forces the inductor current to freewheel around the path consisting of L_o, C_o and the load, and the ultra-fast diode D_1. This effectively transfers the energy stored in the inductor L_o to the capacitor and the load. The output voltage will eventually drop as the capacitor discharges, and the cycle repeats.

Inductor and capacitor sizes are inversely proportional to switching frequency, which accounts for the increasing power density of switched-mode power supplies. A power MOSFET is used instead of a BJT as the pass transistor because of their high frequency capability. Since the pass transistor must not only carry the load current but also the reverse recovery current of diode D_1, an ultra-fast recovery diode or Schottky diode is mandatory.

A typical application is to reduce a standard power supply voltage of 5 V to 1.8 V to power low voltage CMOS logic.

2.12

Step-Down Regulator Waveforms

The voltage and current waveforms of the step-down regulator, assuming there is a very small output voltage ripple, are shown below:

Step-down regulator circuit and waveforms

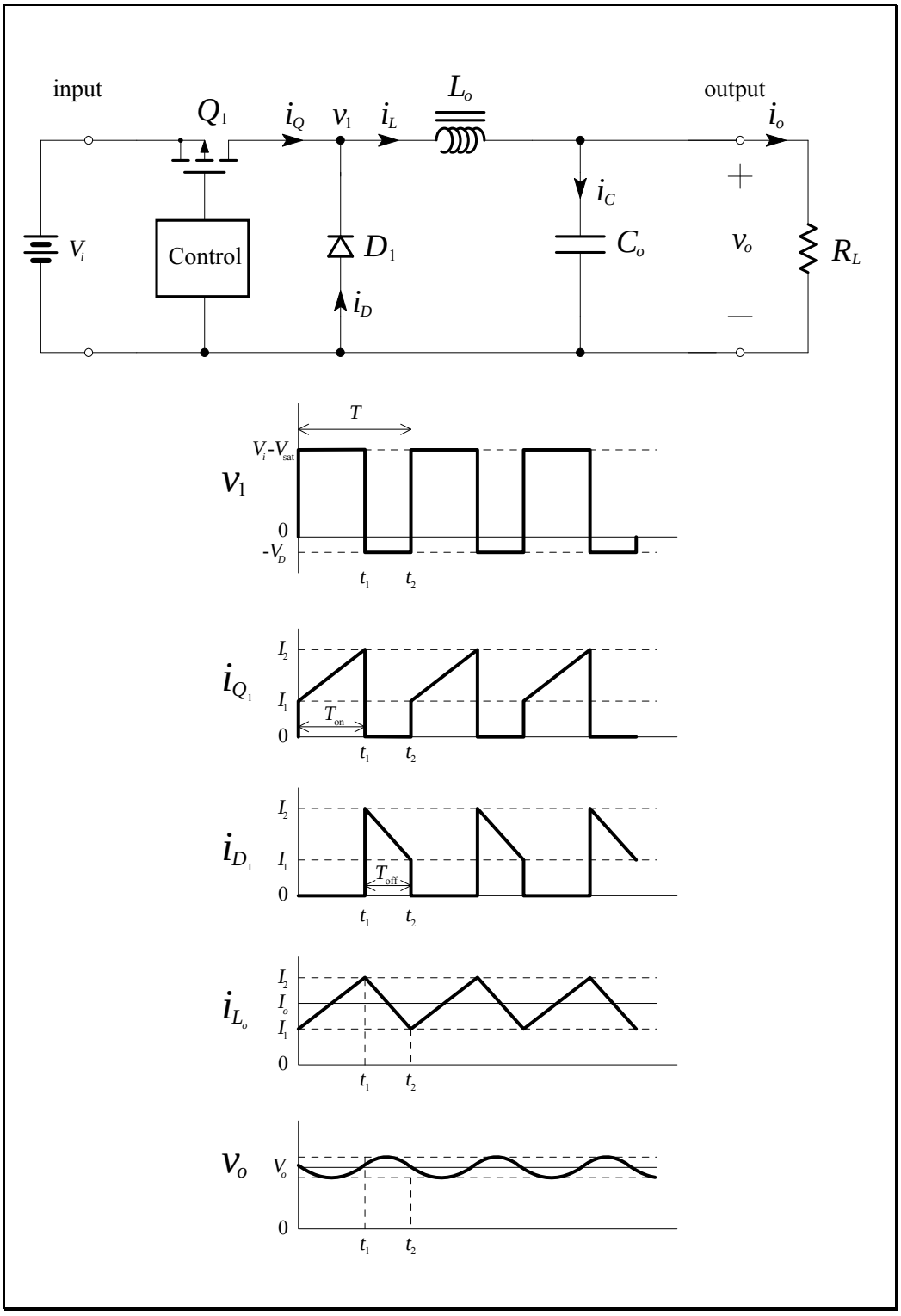


Figure 2.8 – Step-down regulator circuit and waveforms

Step-Down Regulator Analysis

Assume, at time $t = 0^-$, that the transistor is off and the current through the inductor is $i_L = I_1$. When the transistor Q_1 gets turned on by the controller at $t = 0^+$, the voltage v_1 becomes:

$$v_1 = V_i - V_{\text{sat}} \tag{2.4}$$

where V_{sat} is the saturation voltage of the transistor. At this time, the diode is reverse biased and the current through the inductor, i_L, will increase at a rate equal to:

$$\frac{di_L}{dt} = \frac{v_L}{L_o} = \frac{v_1 - v_o}{L_o} \tag{2.5}$$

The current through the inductor continues to increase at this rate as long as the transistor is on and the inductor does not saturate. Assuming that the output voltage over a full cycle does not change significantly, this rate may be considered constant and equal to:

$$\frac{di_L}{dt} = \frac{V_i - V_{\text{sat}} - V_o}{L_o} \tag{2.6}$$

Therefore, the current through the inductor at any instant is given by:

$$i_L = I_1 + \left(\frac{V_i - V_{\text{sat}} - V_o}{L_o} \right) t \tag{2.7}$$

The peak current through the inductor, which is dependent on the on-time of Q_1 is given by:

$$I_2 = I_1 + \left(\frac{V_i - V_{\text{sat}} - V_o}{L_o} \right) T_{\text{on}} \tag{2.8}$$

At the end of the on-time, the transistor is turned off. Since the inductor current cannot change instantaneously, the diode D_1 provides a path for the inductor current, and thus becomes forward biased. The voltage v_1 becomes:

$$v_1 = -V_D \tag{2.9}$$

where V_D is the forward voltage of the diode. The current through the inductor now begins to decay at a rate equal to:

$$\frac{di_L}{dt} = \frac{v_L}{L_o} = \frac{v_1 - v_o}{L_o} = -\left(\frac{V_D + V_o}{L_o}\right) \tag{2.10}$$

The current through the inductor at any instant, while the transistor is off, is therefore given by:

$$i_L = I_2 - \left(\frac{V_D + V_o}{L_o}\right)\left(t - T_{\text{on}}\right) \tag{2.11}$$

Assuming that the current through the inductor reaches I_1 after the time interval T_{off}, then:

$$I_1 = I_2 - \left(\frac{V_D + V_o}{L_o}\right)T_{\text{off}} \tag{2.12}$$

Combining Eqs. (2.8) and (2.12) results in the following relationship between T_{on} and T_{off}:

$$\frac{T_{\text{on}}}{T_{\text{off}}} = \left(\frac{V_D + V_o}{V_i - V_{sat} - V_o}\right) \tag{2.13}$$

If we assume that the diode forward voltage drop and the transistor saturation voltage are negligible compared to the input and output voltages, then:

$$\frac{T_{\text{off}}}{T_{\text{on}}} \approx \frac{V_i - V_o}{V_o} \tag{2.14}$$

and therefore:

$$1 + \frac{T_{\text{off}}}{T_{\text{on}}} \approx 1 + \frac{V_i - V_o}{V_o}$$

$$\frac{T_{\text{on}} + T_{\text{off}}}{T_{\text{on}}} \approx \frac{V_i}{V_o}$$

$$\frac{T}{T_{\text{on}}} \approx \frac{V_i}{V_o} \tag{2.15}$$

The output voltage is therefore:

$$V_o \approx DV_i \tag{2.16}$$

Step-down regulator linear transfer characteristic

where $D = T_{\text{on}}/T$ is the duty cycle.

In the preceding analysis, a number of assumptions were made. For the average output voltage to remain constant, the average output current, $I_o = V_o/R_L$ must be constant. Applying KCL at the output node, it follows that:

$$i_{L_o,\text{avg}} = i_{C_o,\text{avg}} + i_{o,\text{avg}} \tag{2.17}$$

In the steady-state, the average current through the capacitor is zero, and so:

$$i_{L_o,\text{avg}} = i_{o,\text{avg}} = I_o = \frac{V_o}{R_L} \tag{2.18}$$

Thus, the average inductor current is equal to the average output current.

From the i_{L_o} waveform in Figure 2.8, the average output current is:

Average output current

$$I_o = i_{L_o,\text{avg}} = \frac{I_1 + I_2}{2} = \frac{V_o}{R_L} \tag{2.19}$$

The average inductor current depends only on the desired average output voltage and the applied load. The inductor *ripple current* (the AC part of the inductor current) does **not** depend on the load resistance, thus once the switching frequency is set, the ripple current is set. Using Eq. (2.12), the peak-to-peak ripple in the inductor current is given by:

Inductor ripple current

$$\Delta I_{L_o} = I_2 - I_1 \approx \left(\frac{V_o}{L_o}\right) T_{\text{off}} = \frac{(1-D)V_o}{fL_o} \tag{2.20}$$

Examples of inductor current for various loads are shown below:

Inductor currents in continuous mode for various loads

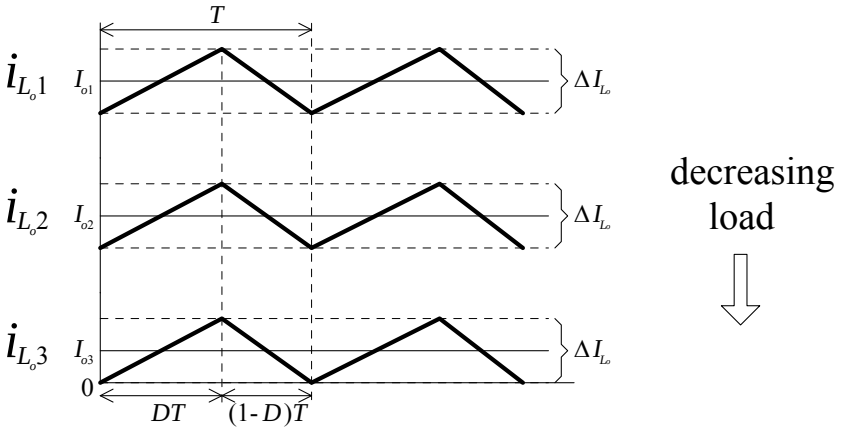
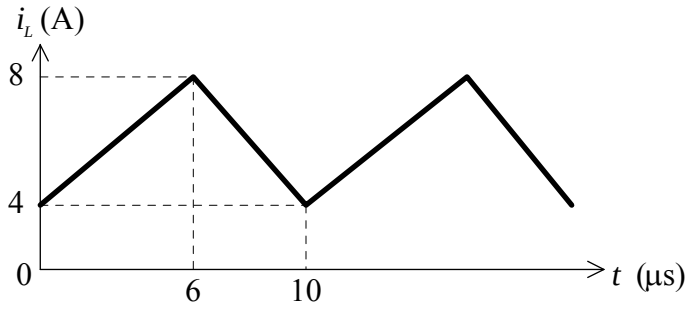


Figure 2.9 – Inductor currents in continuous mode for various loads

As I_o decreases, the minimum inductor current eventually reaches zero. This will transition the circuit into *discontinuous mode* where the linear relationship $V_o = DV_i$ no longer holds. Fortunately, the controller IC employs feedback control, so it will *automatically* find the proper D to achieve the desired output voltage.

Example

Given an ideal step-down regulator with $V_i = 20\text{ V}$ and the following inductor waveform:



Determine:

a) the duty cycle and switching frequency
b) the average output voltage
c) the circuit inductance
d) the load resistance for the operating point pictured
e) the load resistance that transitions the converter to discontinuous mode

a) The duty cycle is given by the ratio of ON time (ramp-up time) to switching period. The switching frequency is the inverse of the switching period so:

$$D = \frac{6}{10} = 0.6 \qquad f = \frac{1}{T} = \frac{1}{10\,\mu\text{s}} = 100\,\text{kHz}$$

b) The ideal input/output relationship for a step-down regulator is $V_o = DV_i$:

$$V_o = 0.6 \times 20\text{ V} = 12\text{ V}$$

c) Rearranging Eq. (2.20) to solve for the inductance yields:

$$L_o = \frac{(1-D)V_o T}{\Delta I_L} = \frac{(1-0.6)\times 12 \times 10 \times 10^{-6}}{8 - 4} = 12\,\mu\text{H}$$

d) The average value of the inductor current is in the centre of the waveform, so it follows that $i_{L_o,\text{avg}} = (4+8)/2 = 6\text{ A}$. Since the average capacitor current must be zero, *the average load current must equal the average inductor current* and:

$$R_L = V_o / I_o = 12/6 = 2\,\Omega$$

e) The transition to discontinuous mode occurs when $I_o = \Delta i_L / 2 = 4/2 = 2\text{ A}$. This occurs when the load resistance equals $R_L = 12/2 = 6\,\Omega$.

2.18

In the analysis it was assumed that the change (ripple) in the output voltage was small in comparison to its average value. This means that the ripple in the load current is small in comparison to its average value, since $v_o = R_L i_o$. KCL at the output gives us $i_{L_o} = i_{C_o} + i_o \approx i_{C_o} + I_o$. This means that most of the inductor ripple current must go through the capacitor. The capacitor current and voltage waveforms are therefore assumed to be:

Output capacitor voltage and current waveforms

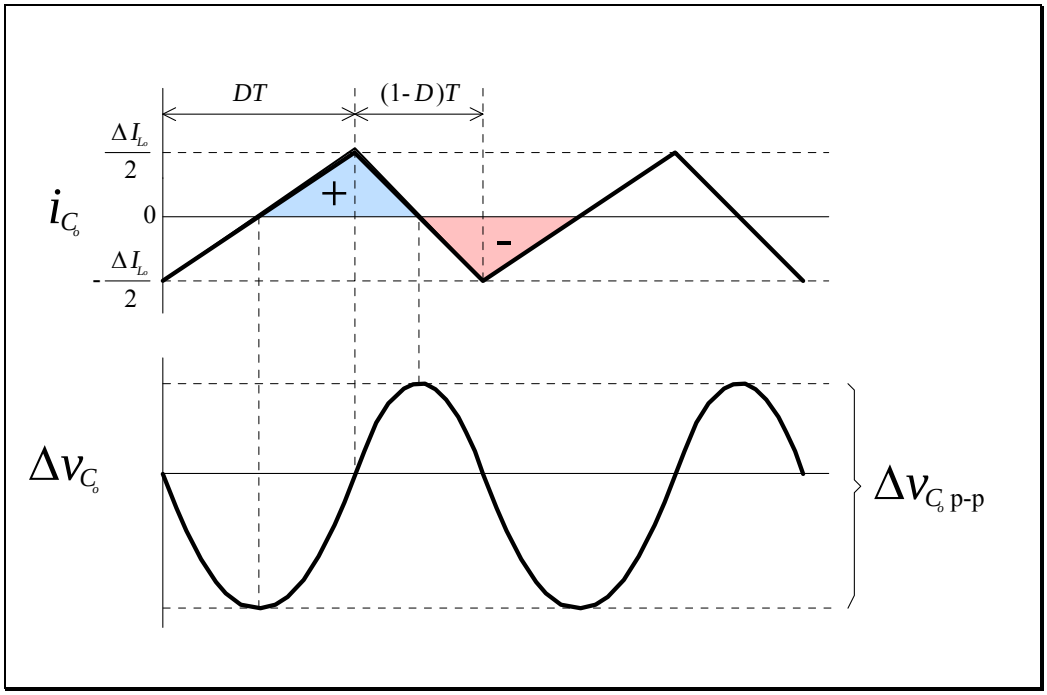


Figure 2.10 – Output capacitor voltage and current waveforms

Note that since the capacitor current is assumed to be piece-wise linear, the capacitor voltage is piece-wise parabolic (since $v_C = \frac{1}{C}\int_0^t i_C dt + v_C(0)$). Also note that since $i_C = C\frac{dv_C}{dt}$, when the capacitor current is positive, the capacitor voltage is increasing and when the capacitor current is negative, the capacitor voltage is decreasing. Also, since the capacitor is an open circuit to DC, it's average (DC) current must be zero. This implies that the area above zero (blue) must be the same as the area below zero (red). Since the positive and negative capacitor current peaks have the same magnitude, we can deduce that the capacitor current is positive for half of the switching period and negative for the other half.

Now since $q = Cv$ for a capacitor, then $\Delta q = C\Delta v$. The change in charge while the current is positive is found by calculating the area under the triangle (blue) whereas the change in voltage will be $\Delta v_{C_o \text{p-p}}$ as shown in Figure 2.10:

$$\begin{aligned}\Delta q &= \int i_{C_o}\, dt \\ &= \frac{1}{2}(base)(height) \\ &= \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta I_{L_o}}{2}\right) \\ &= C_o \Delta v_{C_o \text{p-p}}\end{aligned} \tag{2.21}$$

If we solve for the output peak-to-peak ripple voltage and replace the switching period by one over the switching frequency, we get:

$$V_r = \Delta v_{C_o \text{p-p}} = \frac{\Delta I_{L_o}}{8 f C_o} \tag{2.22}$$

Output peak-to-peak ripple voltage

This tells us, intuitively, that the smaller the output ripple voltage, the larger the capacitance.

Using Eq. (2.20), this can be expressed as:

$$V_r = \frac{(1-D)V_o}{8 f^2 L_o C_o} \tag{2.23}$$

and thus the output peak-to-peak ripple voltage relative to the DC output voltage is:

$$\frac{V_r}{V_o} = \frac{(1-D)}{8 f^2 L_o C_o} \tag{2.24}$$

Output peak-to-peak ripple voltage relative to the DC output voltage

The RMS value of the ripple current through the capacitor can be determined from first principles using the current waveform shown in Figure 2.10. Omitting the details, the RMS value is:

$$I_{C_o RMS} = \frac{I_{pk}}{\sqrt{3}} = \frac{\Delta I_{L_o} / 2}{\sqrt{3}} = \frac{\Delta I_{L_o}}{\sqrt{12}} \tag{2.25}$$

Example

Given the step-down regulator from the previous example, with $V_o = 12\,\text{V}$, if we impose a maximum output voltage ripple of 1% of the DC value, determine the required capacitance.

From Eq. (2.24), we get:

$$\begin{aligned} C_{o\min} &= \frac{(1-D)}{8 f^2 L_o (V_r / V_o)} \\ &= \frac{(1-0.6)}{8 \times (100 \times 10^3)^2 \times 12 \times 10^{-6} \times (0.01)} \\ &= \frac{0.4}{9600} \\ &= 41.67\,\mu\text{F} \end{aligned}$$

Alternatively, we can use Eq. (2.22) with $V_r = 0.01 \times 12 = 0.12\,\text{V}$ and $\Delta I_{L_o} = 4\,\text{A}$, and get the same result.

This is not a standard value of capacitance, so we would scale up to the next largest standard value, $47\,\mu\text{F}$. The RMS current that it is expected to handle is:

$$I_{C_o RMS} = \frac{\Delta I_{L_o}}{\sqrt{12}} = \frac{4}{\sqrt{12}} = 1.155\,\text{A}$$

We would carefully choose the capacitor so that it can handle this RMS current.

Efficiency

The efficiency of the step-down regulator is:

$$\eta = \frac{P_o}{P_i} \tag{2.26}$$

where $P_o = V_o I_o$ is the average output power and $P_i = V_i I_i$ is the average input power. The average input current can be calculated from the i_Q waveform in Figure 2.8. Using the trapezoidal rule to calculate the area, we get:

$$I_i = i_{Q\text{av}} = \frac{I_1 + I_2}{2}\frac{T_{\text{on}}}{T} = I_o \frac{T_{\text{on}}}{T} \tag{2.27}$$

Using Eq. (2.27) the efficiency is:

$$\begin{aligned} \eta &= \frac{V_o I_o}{V_i I_i} \\ &= \frac{V_o I_o T}{V_i I_o T_{\text{on}}} \\ &= \frac{V_o}{V_i}\left(\frac{T_{\text{on}} + T_{\text{off}}}{T_{\text{on}}}\right) \end{aligned} \tag{2.28}$$

Using Eq. (2.13) the efficiency is therefore:

$$\eta = \frac{V_o}{V_i}\left(\frac{V_i - V_{sat} + V_D}{V_D + V_o}\right) \tag{2.29}$$

Step-down regulator efficiency

As the forward drops in the diode and transistor decrease, the efficiency of the system is improved. With variations in input voltage, the efficiency remains relatively constant. The above calculation for efficiency did not take into account the quiescent power dissipation of the controller IC, the switching losses in the diode and transistor, or losses in the inductor – all of which reduce the efficiency.

Discontinuous Mode

The current waveform of the output inductor in Figure 2.8 is shown as a characteristic ramp-on-a-step waveform. The current amplitude at the centre of the ramp is the average value, and is equal to the DC output current, I_o. At a load current of half the peak-to-peak magnitude of the ramp, the lower point of the ramp just touches zero. If the load current is further reduced, there will be a period when the inductor current remains at zero for a longer period and the step-down regulator enters into the "discontinuous current" operating mode:

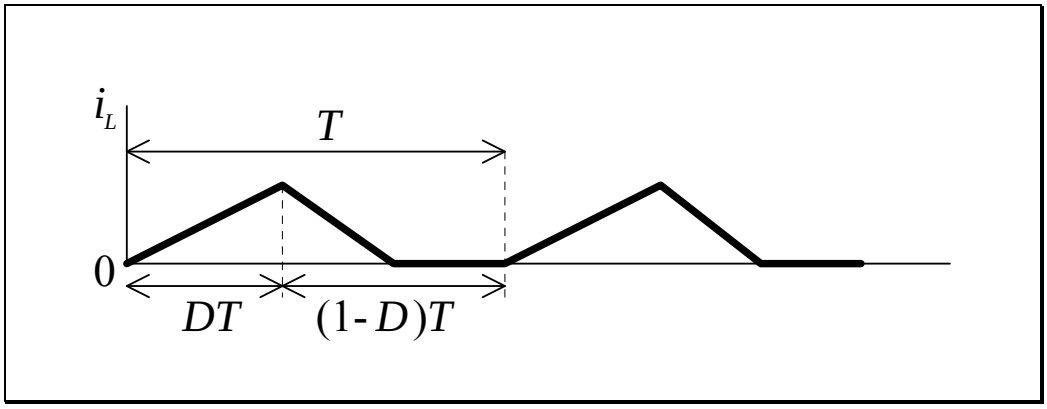


Figure 2.11 – Inductor current in discontinuous mode

This is an important transition because a change occurs in the current and voltage waveforms and in the closed-loop behaviour of the SMPS. The transfer function changes drastically and the linear equation for the output voltage, $V_o = DV_i$, no longer applies. To maintain a constant output voltage, the duty cycle $D = T_{\text{on}}/T$ must change with reducing load current. Hence, the control loop must "work harder", and the transient performance will be degraded.

With no rate-of-change of current in the output inductor, its voltage will be zero, and the output voltage will seek to appear at the drain of Q_1. However, the sudden transition results in a decaying voltage "ring", at a frequency determined by L_o and the distributed capacitance seen looking into the cathode of D_1 and the drain of Q_1. Although not damaging, in the interest of RFI reduction, either steps should be taken to suppress the ringing, or the discontinuous mode should be avoided altogether by designing the inductor so that it remains in the continuous mode for the full range of expected (but limited) load currents.

Example

An inductor for a step-down regulator will be chosen so that the current remains continuous if the DC output current stays above a specified minimum value (typically this is chosen to be around 10% of the rated load current, i.e. $I_1 = 0.1I_{on}$, where I_{on} is the *nominal* output current).

The range of the inductor current ramp (refer to the waveform in Figure 2.8) is $I_2 - I_1$. Since the onset of the discontinuous mode occurs at a DC current of half this amplitude, then:

$$I_{o\min} = (I_2 - I_1)/2 \quad \text{or} \quad I_2 - I_1 = 2I_{o\min}$$

Also, from Eq. (2.8):

$$I_2 - I_1 = \left(\frac{V_i - V_{\text{sat}} - V_o}{L}\right)T_{\text{on}}$$

Combining the two, we have:

$$L = \left(\frac{V_i - V_{\text{sat}} - V_o}{2I_{o\min}}\right)T_{\text{on}}$$

Now since:

$$T_{\text{on}} \approx \frac{V_o T}{V_i}$$

then the minimum inductor value to avoid discontinuous current at $I_{o\min}$ is:

$$L = \left(\frac{V_i - V_{\text{sat}} - V_o}{2I_{o\min}}\right)\frac{V_o T}{V_i}$$

The inductor current will swing $(I_2 - I_1)/2$ around its centre value. If the above formula for L is used then $(I_2 - I_1)/2 = I_{o\min}$. When operating at nominal load current I_{on}, the peak current will be:

$$I_{2n} = I_{on} + I_{o\min}$$

and so the inductor must be designed so that it does not significantly saturate at a current of at least this value.

Step-Up (Boost) Regulator

A step-up regulator is capable of boosting the input voltage:

Step-up regulator circuit and waveforms

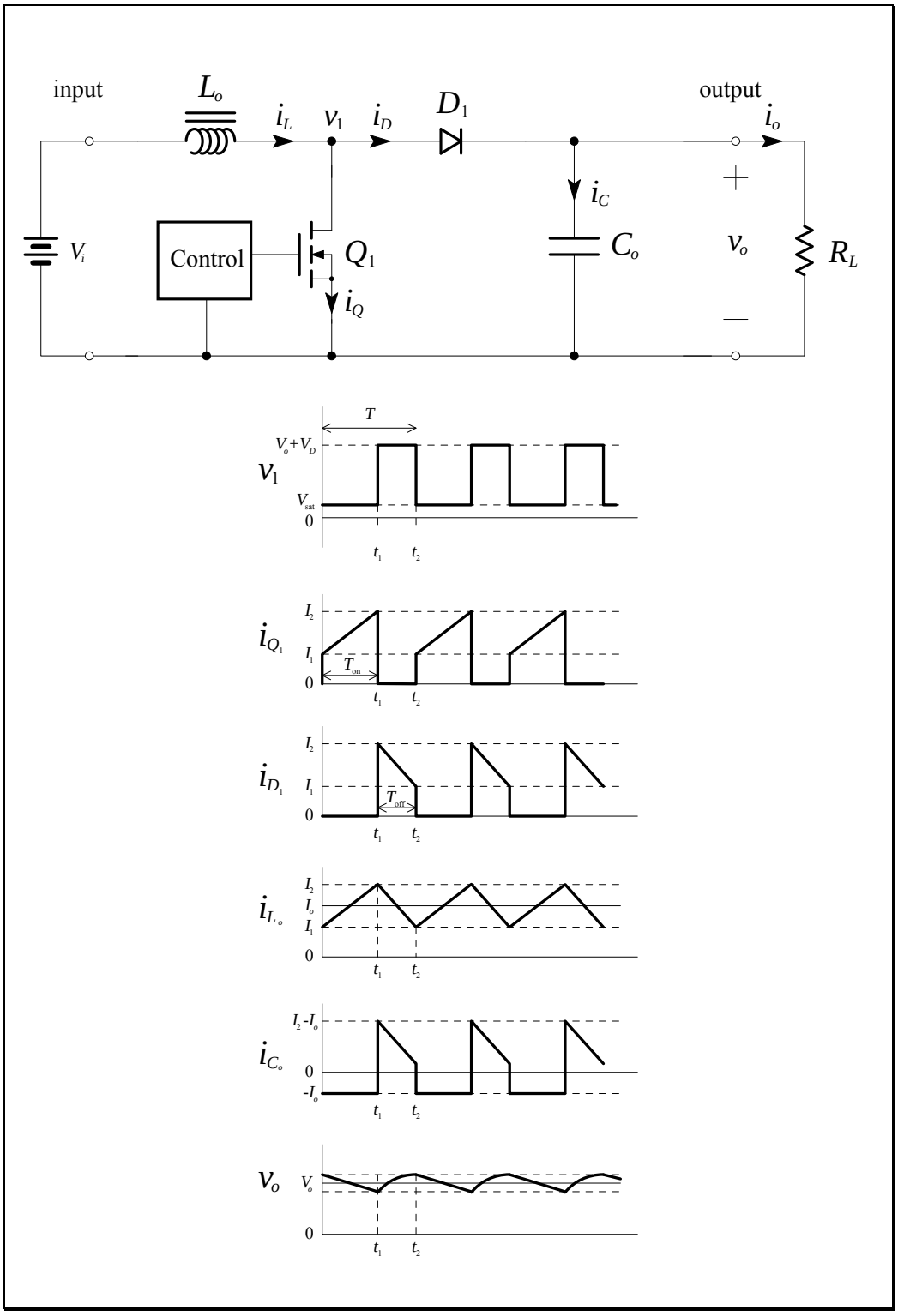


Figure 2.12 – Step-up regulator circuit and waveforms

Applications for this circuit would be to increase 5V battery sources to 12V for interface circuits or even to 150V for electro-luminescent displays.

The concept of operation of this circuit is the same as for the step-down regulator, namely to transfer the energy stored in the inductor into the capacitor and load. The inductor current can ramp up quickly when the transistor switch is closed since the full input voltage is applied to it. The transistor is turned off at time t_1, after a duration of T_{on}, which forces the inductor current to charge up the capacitor through the ultra-fast diode D_1.

Analysis of the circuit proceeds in a manner similar to that undertaken for the step-down regulator. It can be shown that:

$$\frac{T_{\text{on}}}{T_{\text{off}}} = \left(\frac{V_o + V_D - V_i}{V_i - V_{sat}} \right) \tag{2.30}$$

and therefore the transfer function is:

$$V_o \approx \left(\frac{1}{1 - D} \right) V_i \tag{2.31}$$

Step-up regulator transfer characteristic

Therefore the output voltage is greater than the input voltage, and varies inversely with the duty cycle. The PWM IC measures the output voltage v_o and controls the duty cycle to achieve the desired output voltage.

The efficiency of the step-up regulator, ignoring the quiescent power dissipation of the controller IC, the switching losses in the diode and transistor, and the losses in the inductor, is given by:

$$\eta = \frac{V_i - V_{sat}}{V_i} \left(\frac{V_o}{V_o + V_D - V_{sat}} \right) \tag{2.32}$$

Step-up regulator efficiency

Again, as the forward drops in the diode and transistor are reduced, the efficiency improves.

2.26

Inverting Regulator

An inverting regulator is a switching circuit which produces an output voltage with the opposite polarity of the input voltage:

Inverting regulator circuit and waveforms

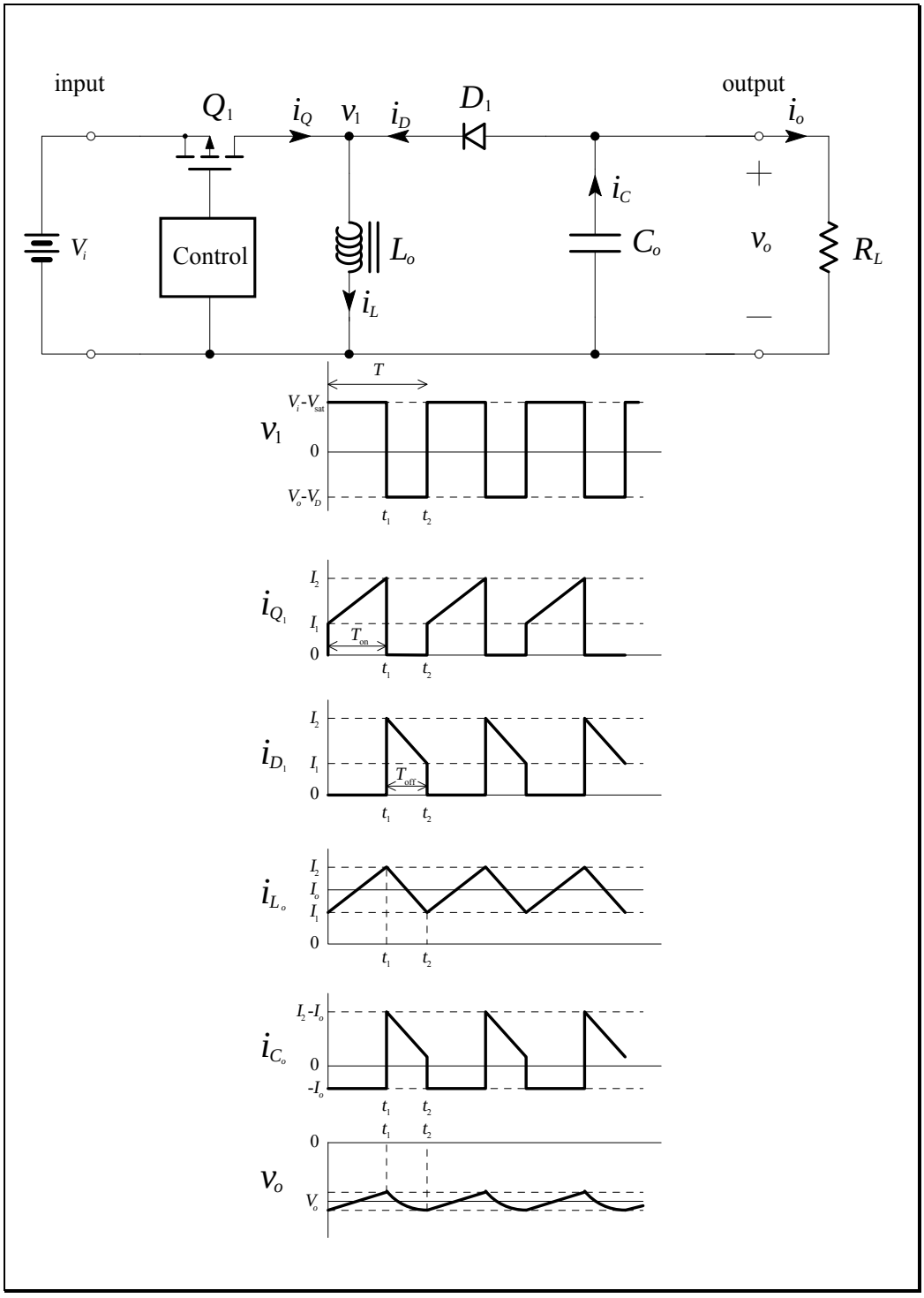


Figure 2.13 – Inverting regulator circuit and waveforms

This circuit works in the same fashion as the step-up converter but has achieved the voltage inversion by exchanging positions of the transistor and inductor. The circuit is also known as a buck-boost regulator since the absolute magnitude of the output voltage can be higher or lower than the input voltage, depending upon the ratio of on-time to off-time of the pass transistor.

Analysis of the circuit proceeds in a manner similar to that undertaken for the step-down regulator. It can be shown that:

$$\frac{T_{\text{on}}}{T_{\text{off}}} = \left(\frac{V_D - V_o}{V_i - V_{sat}} \right) \tag{2.33}$$

and therefore the transfer function is:

$$V_o \approx \left(\frac{-D}{1-D} \right) V_i \tag{2.34}$$

Inverting regulator transfer characteristic

Therefore the output voltage is always negative, but it can be greater or smaller in magnitude than the input voltage. The PWM IC measures the output voltage v_o and controls the duty cycle to achieve the desired output voltage.

The efficiency of the inverting regulator, ignoring the quiescent power dissipation of the controller IC, the switching losses in the diode and transistor, and the losses in the inductor, is given by:

$$\eta = \frac{V_i - V_{sat}}{V_i} \left(\frac{V_o}{V_o - V_D} \right) \tag{2.35}$$

Inverting regulator efficiency

Again, as the forward drops in the diode and transistor are reduced, the efficiency improves.

Single-Ended Primary-Inductor Converter (SEPIC)

A single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter allowing the voltage at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle of the control transistor.

SEPIC regulator circuit

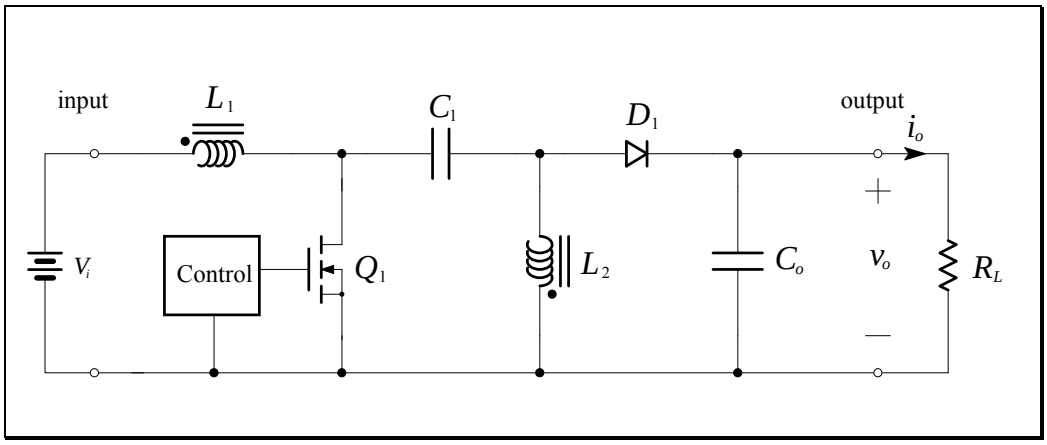


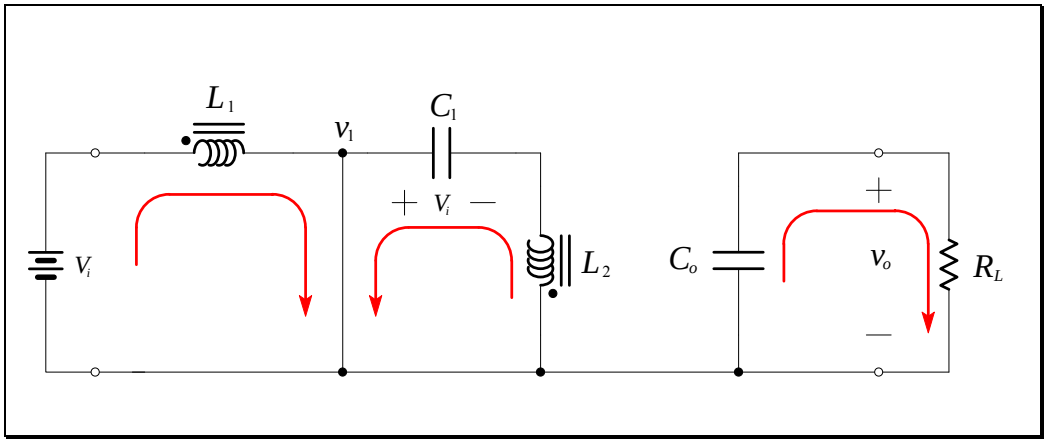
Figure 2.14 – Single-ended primary-inductor converter (SEPIC)

A SEPIC is similar to a traditional buck-boost converter, but has the advantages of:

- non-inverted output
- isolation between its input and output (provided by a capacitor in series)
- true shutdown mode: when the control transistor is turned off, the output drops to 0 V.

SEPICs are useful in applications in which a battery voltage can be above and below that of the regulator's intended output. For example, a single Li-ion battery typically discharges from 4.2 volts to 3 volts; if a desired constant output voltage of 3.3 V is desired, then the SEPIC would be effective.

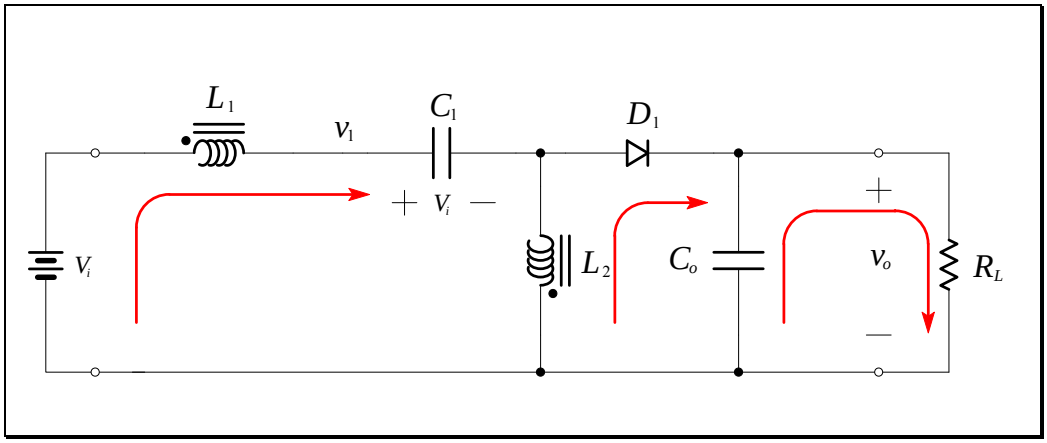
The current paths in a SEPIC during the switch's on-time are shown below:



SEPIC current paths during the switch's on-time

Figure 2.15 – SEPIC current paths during the switch's on-time

The current paths in a SEPIC during the switch's off-time are shown below:



SEPIC current paths during the switch's off-time

Figure 2.16 – SEPIC current paths during the switch's off-time

The two inductors L_1 and L_2 can be independent but can also be wound on the same core since identical voltages are applied to L_1 and L_2 throughout the switching cycle. By making $L_1 = L_2$ and winding them on the same core the input ripple is reduced along with cost and size.

Selection of Components

Switching Components

The designer should be fully aware of the capabilities and limitations of power transistors used in switching applications. Transistors in linear applications operate around a quiescent point; whereas in switching applications operation is fully on or fully off. Transistors must be selected and tested to withstand the unique stress caused by this mode of operation.

Parameters such as current and voltage ratings, secondary breakdown ratings, power dissipation, saturation voltage and switching times critically affect transistor performance in switching applications. Similar parameters are important in diode selection, including voltage, current, and power limitations, as well as forward voltage drop and switching speed.

Initial selection can begin with voltage and current requirements. Voltage ratings of the switching transistor and diode must be greater than the maximum input voltage, including any transient voltages that may appear at the input of the switching regulator. Transistor saturation voltage $v_{DS(\text{sat})}$ and diode forward voltage v_D at full load output current should be as low as possible to maintain high operating efficiency. The transistor and diode should be selected to handle the required maximum peak current and power dissipation.

Good efficiency requires fast switching diodes and transistors.

Diodes

For all but the highest voltage designs, Schottky diodes are the recommended choice. They are available in breakdown voltages up to ~100 V. The lower forward voltage drop of Schottky diodes, compared to silicon diodes, reduces the power dissipation considerably. The effectively zero reverse-recovery time also prevents switching losses in the diode.

Schottky diodes are also available with ultralow forward voltage drop. These are only available in breakdown voltages up to ~40 V, and will cost a bit more, but will reduce power dissipation in the diode even further.

When selecting a diode, one must consider the forward voltage drop, breakdown voltage, average forward current, and maximum power dissipation. Choose a device with a forward drop as low as possible, but be sure to use numbers from the data sheet that reflect the forward voltage drop at the current that will be seen in the design. Often, forward voltage drop will increase greatly with increasing forward current. A higher forward voltage drop will cause greater power dissipation in the device. This, in turn, will decrease converter efficiency and may overheat the diode.

Diodes have a negative forward voltage temperature coefficient. As the temperature of the diode rises, the forward voltage drop will decrease, hence decreasing the power dissipated within the device. However, because of this effect, the paralleling of diodes to share current is not recommended, as one diode will tend to dominate and hog all the current in a paralleled system.

The diode’s breakdown voltage should be rated above the voltages in the system. The forward current rating should be greater than the designed RMS current for the circuit’s inductor. Also, the diode needs to be able to dissipate enough power to avoid overheating. Choose a device with a maximum power dissipation specification larger than the design requirements.

Inductors

Inductors are made by winding wire around a core. In switching applications, selecting the proper core requires consideration of two important factors.

Firstly, the core must provide the desired inductance without saturating magnetically at the maximum peak current. In this respect, each core has a specific energy storage capability $w_{L(\text{sat})} = \frac{1}{2} L i_{\text{sat}}^2$.

Secondly, the window area for the core winding must be as small as possible, so that it is inexpensive, but it must also permit the number of turns necessary to obtain the required inductance with a wire size that has acceptable DC losses in the winding at maximum peak current. In switching regulator applications, power dissipation in the inductor is almost entirely due to DC losses in the winding. Each core has a specific power dissipation capability that will result in a temperature rise. This temperature rise plus the ambient temperature must not exceed the Curie temperature of the core.

Cores use ferrite material which has a low loss at the high switching frequencies and are capable of high flux densities.

One procedure for designing the inductor is as follows:

1. Calculate the inductance L and the peak current I_{peak} for the application. The required energy storage capability of the inductor can now be defined as $w_{L(\text{req})} = \frac{1}{2} L I_{\text{peak}}^2$.
2. Determine the maximum energy storage capability of a selected core, $w_{L(\text{sat})} = \frac{1}{2} L i_{\text{sat}}^2$ and ensure that $w_{L(\text{sat})} > w_{L(\text{req})}$.
3. Calculate the number of turns N required for the specified inductance L, and hence determine the power dissipation of the wire due to DC resistance. The power dissipation should be less than the maximum permissible power dissipation of the core. If the power losses are unacceptable, a larger core or one with a higher permeability is required.

Several design cycles are usually required to optimize the inductor design.

Choosing the right value of inductance for a SMPS design is not a simple calculation, but most designs will work within a fairly wide range of inductance values. Datasheets for switching ICs will generally provide tables, or a range of preferred values, for use at particular switching frequencies.

Benefits of lower value inductors include:

- Lower DC resistance
- Higher saturation current
- Higher di/dt
- Faster switching frequency
- Better transient response

Benefits of higher value inductors include:

- Lower ripple current
- Lower core losses
- Lower RMS currents in the switching transistors
- Lower capacitance required to meet output ripple specification

A relatively new player in the inductor family is the multilayer chip inductors. These chip inductors are available in very small physical sizes (0805) and allow for a very small overall design. The inductance values are currently available up to 4.7 μH, so they generally lend themselves to higher switching frequency designs. The small size also limits the current handling capacity, approximately 1.5 A, so they are not viable for higher power designs. They are lower cost, smaller size, and have lower DC resistance than standard wire wound inductors.

Shielded inductors are more expensive and have a lower saturation current (for the same physical size and value) than their non-shielded counterparts, but they greatly reduce EMI. It is almost always worth using shielded inductors to help avoid any EMI issues with a design. This is especially true when using higher switching frequencies.

Capacitors

In SMPS designs, capacitors perform the functions of energy storage and filtering. As with all real devices, there are capacitor parasitics that a designer must be aware of. In the context of energy storage and filtering, the two most important parasitics are equivalent series resistance (ESR) and equivalent series inductance (ESL). The figure below illustrates the capacitors in a step-down converter design.

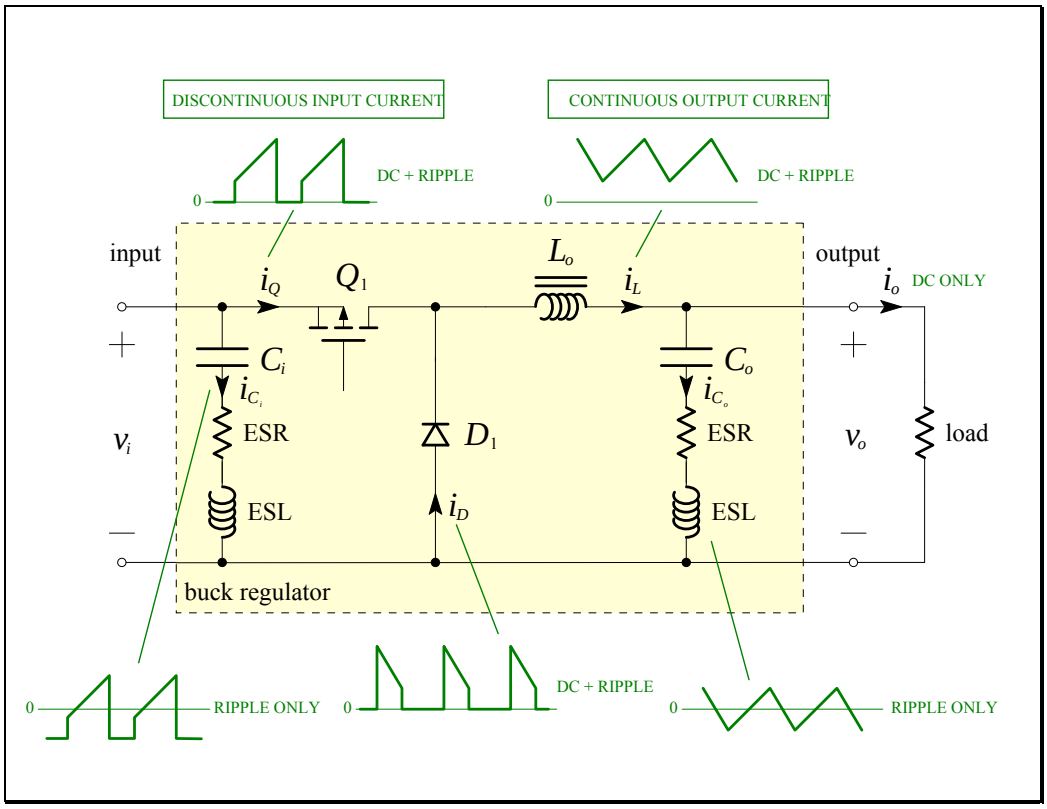


Figure 2.17 – Capacitor functions in a step-down converter design

The input capacitor will see large discontinuous ripple currents. This capacitor needs to be rated for high ripple currents (low ESR) and low inductance (ESL). If the input capacitor ESR is too high, this will cause RI^2 power dissipation within the capacitor. This will reduce converter efficiency and potentially overheat the capacitor. The discontinuous nature of the input current will also interact with the ESL, causing voltage spikes on the input. This will introduce unwanted noise into the system. The input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. Be sure to specify surge-resistant capacitors!

The output capacitor in a step-down converter will see continuous ripple currents which are generally low. The ESR should be kept low for best efficiency and load transient response.

It may be wise to use several capacitors in parallel to build a larger capacitance. Capacitance will add in parallel, whereas ESR and ESL will decrease. By using two (or more) capacitors in parallel, you can get a larger capacitance and lower inductance and resistance. This is often the only way to get the required high capacitance and low ESR to meet design requirements.

Aluminium electrolytic capacitors represent the best cost/μF of all the options. The chief disadvantage of aluminium electrolytic capacitors is the high ESR, which can be on the order of several ohms. Be sure to use switching type capacitors, as these will have lower ESR and ESL than their general-purpose counterparts. Aluminium electrolytic capacitors also rely on an electrolyte which can dry out over time, thus reducing their lifespan.

Tantalum capacitors use a tantalum powder as the dielectric. They offer large values in smaller packages than an equivalent aluminium capacitor, though at higher cost. ESR tends to be in the 100 mΩ range, lower than aluminiums. Since they do not use a liquid electrolyte, their lifespan is longer than the aluminium electrolytic type. For this reason, they are popular in high reliability applications. Tantalum capacitors are sensitive to surge currents and will sometimes require series resistance to limit the inrush currents. Be careful to stay within the manufacturers recommended surge current ratings, as well as voltage ratings. The failure mode of tantalums capacitors can be a burn out with flame.

The Multi-Layered Ceramic Capacitor (MLCC) offers extremely low ESR (<10 mΩ) and ESL (<1 nH) in a small surface-mount package. MLCCs are available in sizes up to 100 μF, though the physical size and cost will increase for values >10 μF. Be aware of the voltage rating of MLCCs, as well as the dielectric used in their construction. The actual capacitance will vary with applied voltage, and the variation can be very large depending on the dielectric chosen. X7R type dielectric offers the best performance and is highly recommended.

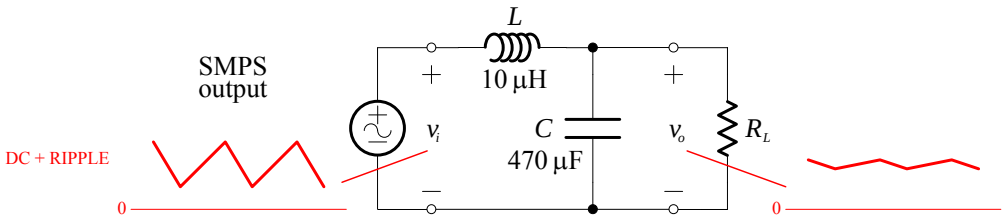
2.36

Output Filters

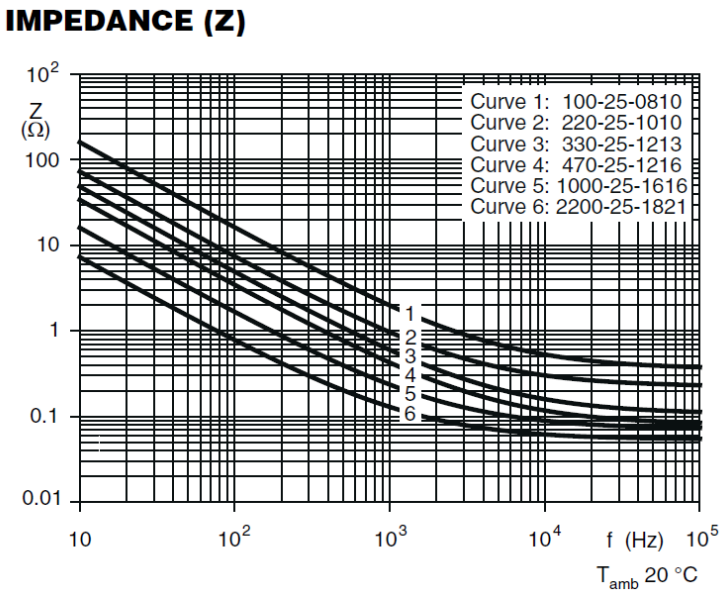
Switched-mode power supplies are "noisy" in the sense that the output ripple voltage fluctuates at the switching frequency. It is sometimes necessary to provide an additional output filter in the form of an *LC* lowpass filter to further attenuate the ripple voltage.

Example

An *LC* lowpass filter is applied to the output of a SMPS:

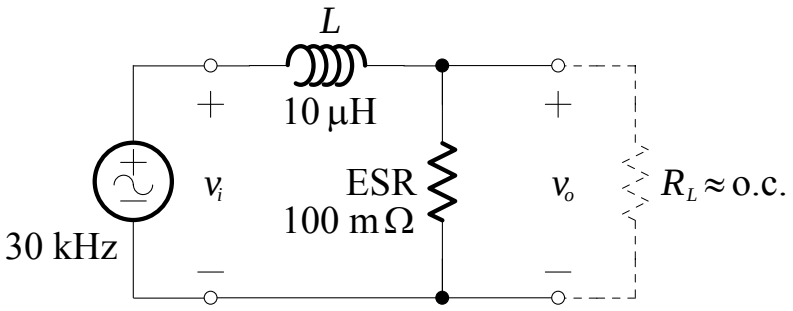


The switching frequency is 30 kHz. The switching frequency ripple (i.e. the fundamental component of the ripple) is the predominant ripple component in a SMPS. From the capacitor datasheet (Curve 4), at a frequency of 30 kHz we can model the capacitor as an equivalent series resistance (ESR) of 100 mΩ, which effectively "shorts" the load resistance.



Since the impedance curve is horizontal from about 10 kHz, we know we are nearing the self-resonance frequency of the capacitor, and so a simple ESR model is appropriate. At frequencies above 100 kHz, the capacitor will turn inductive.

The attenuation provided by this *LC* network at 30 kHz may now be easily calculated, since the capacitor looks predominantly resistive and forms a simple divider network with the series impedance of the inductor:



The ratio of the output voltage ripple to the input voltage ripple is:

$$\frac{\mathbf{V}_o}{\mathbf{V}_i} = \frac{\text{ESR}}{\text{ESR} + jX_L}$$

At 30 kHz, X_L will be:

$$X_L = 2\pi fL = 2\pi \times 30 \times 10^3 \times 10 \times 10^{-6} = 1.885\,\Omega$$

Hence, the magnitude response is:

$$\left|\frac{\mathbf{V}_o}{\mathbf{V}_i}\right| = \frac{0.1}{|0.1 + j1.885|} = 0.05298$$

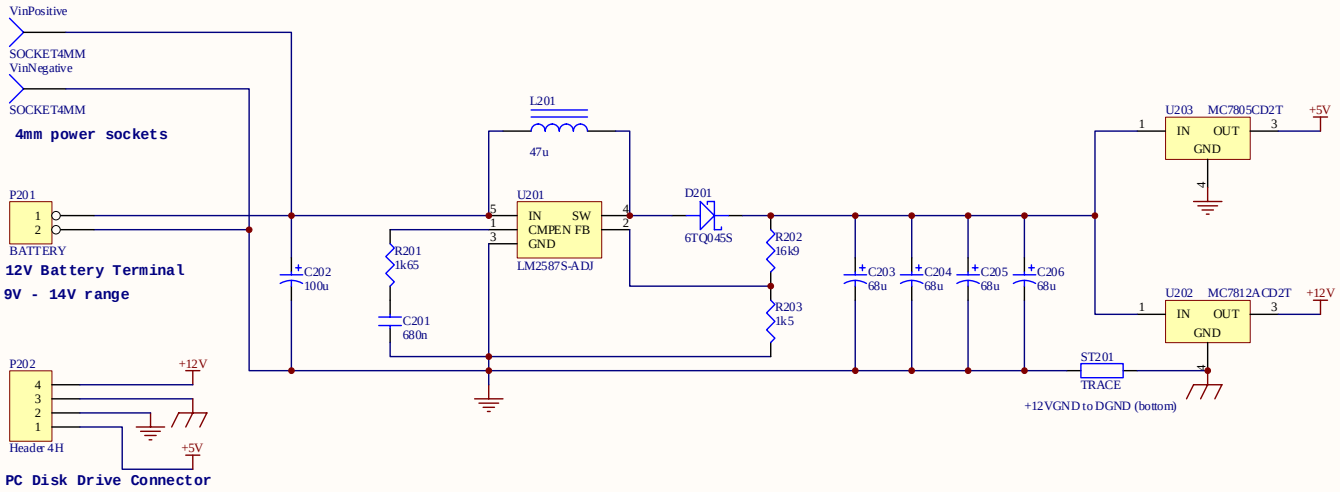
Thus, the filter provides a ripple rejection of -25.52 dB at the switching frequency (and not necessarily more at higher frequencies due to the fact that the capacitor becomes inductive after its self-resonance frequency is reached).

References

National Semiconductor*: LM78S40 Switching Voltage Regulator Applications*, *Application Note 711*, Texas Instruments, March 2000.

Pressman, A., Billings, K. & Morey, T.*: Switching Power Supply Design*, 3rd *Ed*., McGraw-Hill, 2009.

Watkins, T.: *Selecting the Right Passive and Discrete Components for Top System Performance;* Technical Article MS-2208, Analog Devices, 2011.



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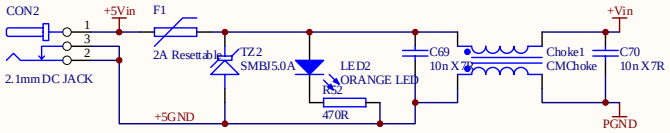
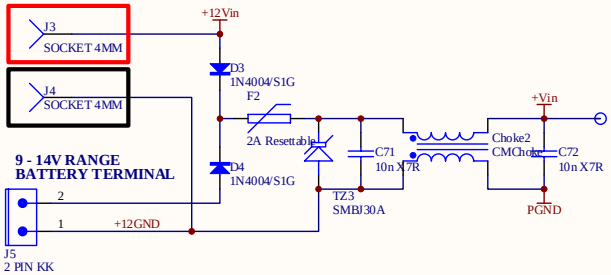
Size: A3	Number: **Power**	Revision: **1.0**
Date: 1/04/2009	Sheet 4 of 4	
File: C:\Projects\ModCon\Power.SCHDOC	Drawn By: PMcL	

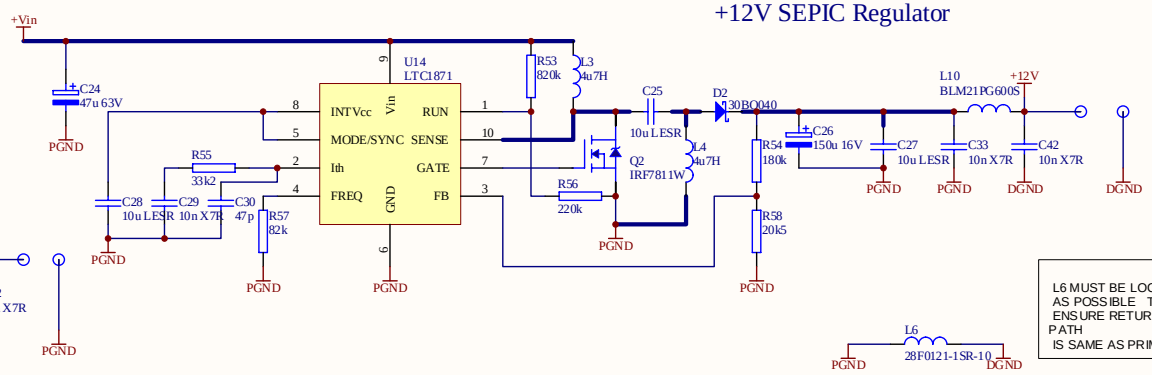
5V Regulated Input



Power Supply Input

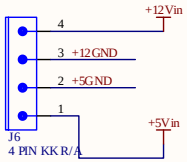


+12V SEPIC Regulator

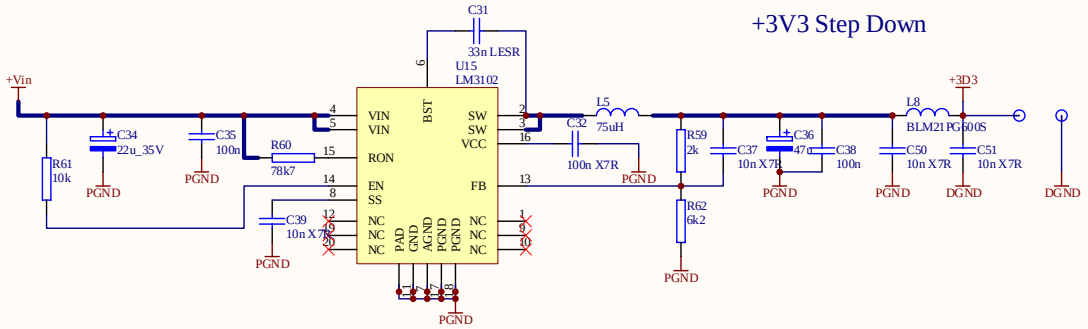


L6 MUST BE LOCATED AS CLOSE AS POSSIBLE TO L10 ,L8. ENSURE RETURN CURRENT PATH IS SAME AS PRIMARY

PC Power

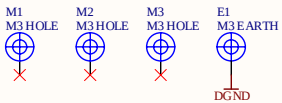


+3V3 Step Down



FeedBack track must clear inductor to avoid induced artifacts

Connections to switching supplies to be as short and as thick as possible



Note: Fitting options

Section	BACKPLANE	STANDALONE	MROVER	PC
5V Regulated Input		FIT		
12V Power Supply Input			FIT	
+12V SEPIC Regulator	FIT		FIT	
PC Power				FIT

Project: **ModCon**	Title: **POWER**		
	Size: A3	Number: 2	Revision: 1A
	Print Date: 1/04/2009		Sheet 2 of 8
	File: ModCon POWER.SchDoc		
	Drawn: Joe TRINH	Approved: PMcL	Approved Date: dd/mm/yyyy