Logic Families/Objectives

- Digital Logic Voltage and Current Parameters
  - Fan-out, Noise Margin, Propagation Delay
- TTL Logic Family
- TTL Logic Family Evolution
- ECL
- CMOS Logic Families and Evolution
- Logic Family Overview

Logic Families/Level of Integration

- SSI <12 gates/chip
- MSI 12..99 gates/chip
- LSI ..1000 gates/chip
- VLSI …10k gates/chip
- ULSI …100k gates/chip
- GSI …1Meg gates/chip

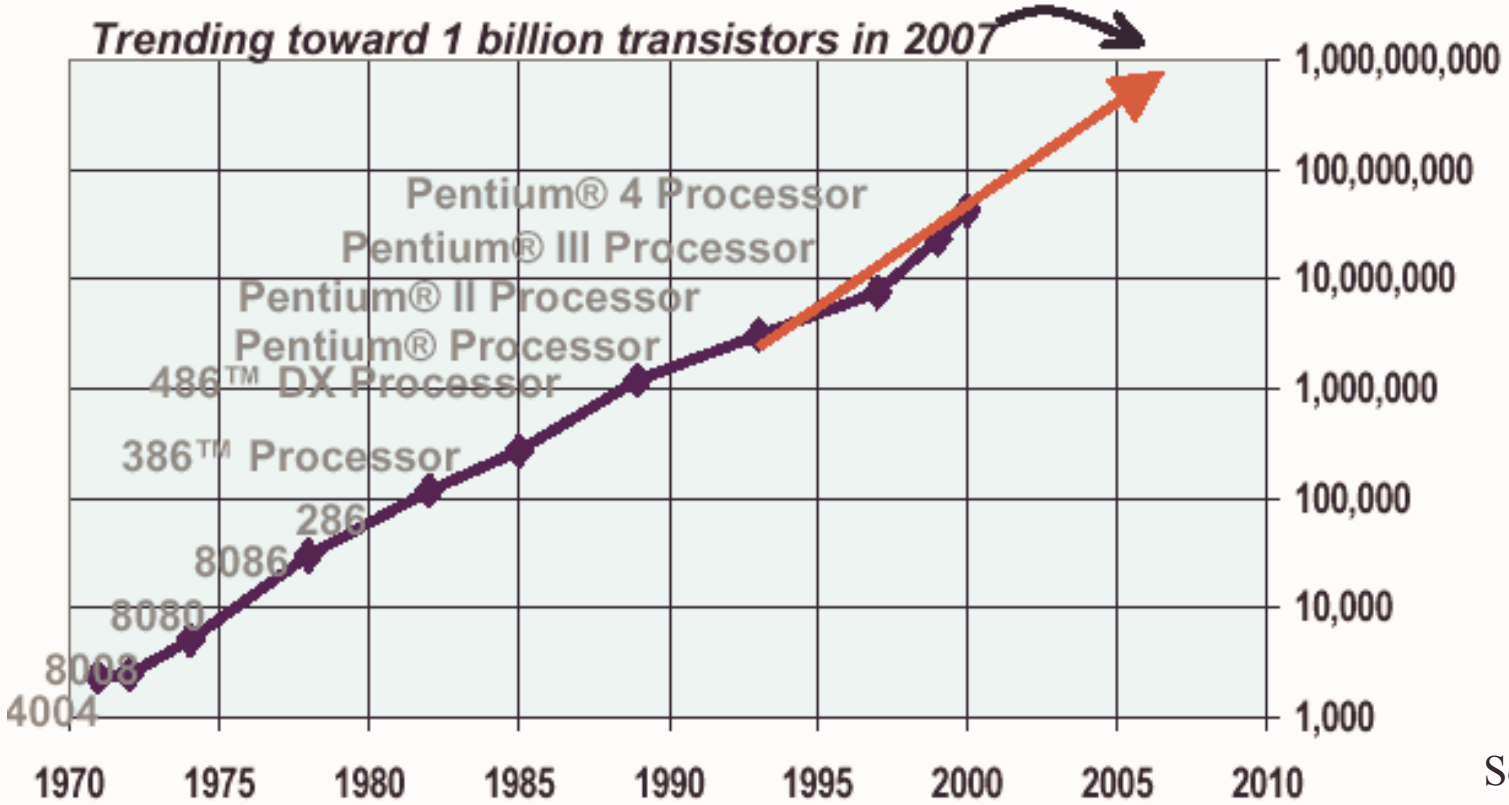
Note: Ratio gate count/transistor count is roughly 1/10

Level of integration ever increasing, because of
- cost
- speed
- size
- power
- reliability

Limits of integration:
- packaging
- power dissipation
- inductive and capacitive components
- flexibility
- critical quantity

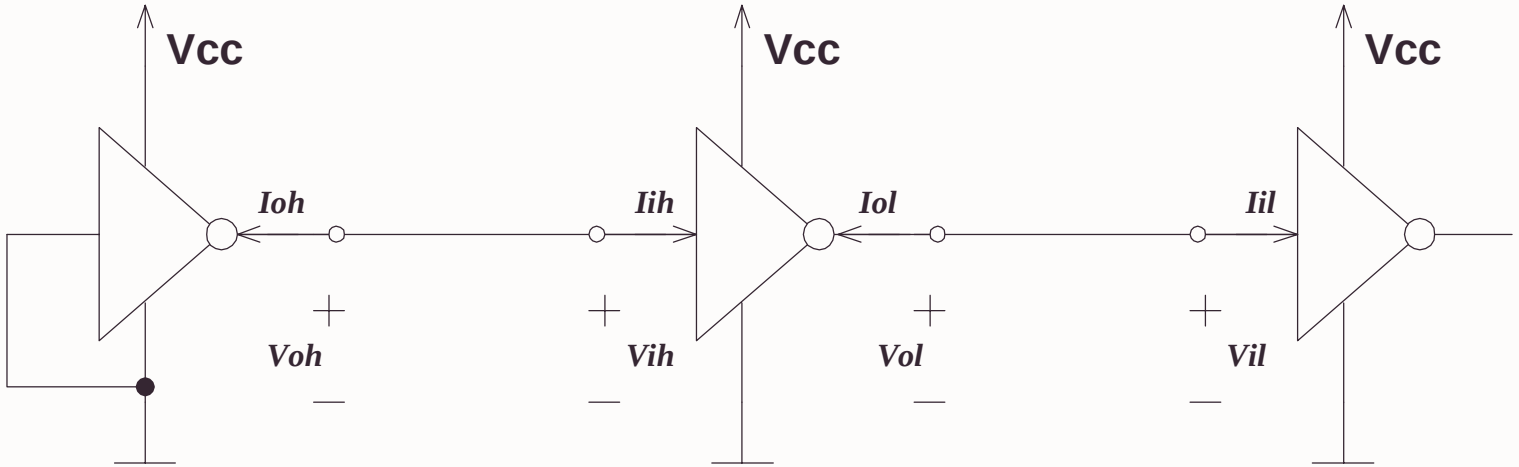
Logic Families/Level of Integration

– Remember: Gordon Moore, 1975. Predictions:
  - Mosfet device dimensions scale down by a factor of 2 every 3 years
  - #transistors/chip double every 1-2 years.



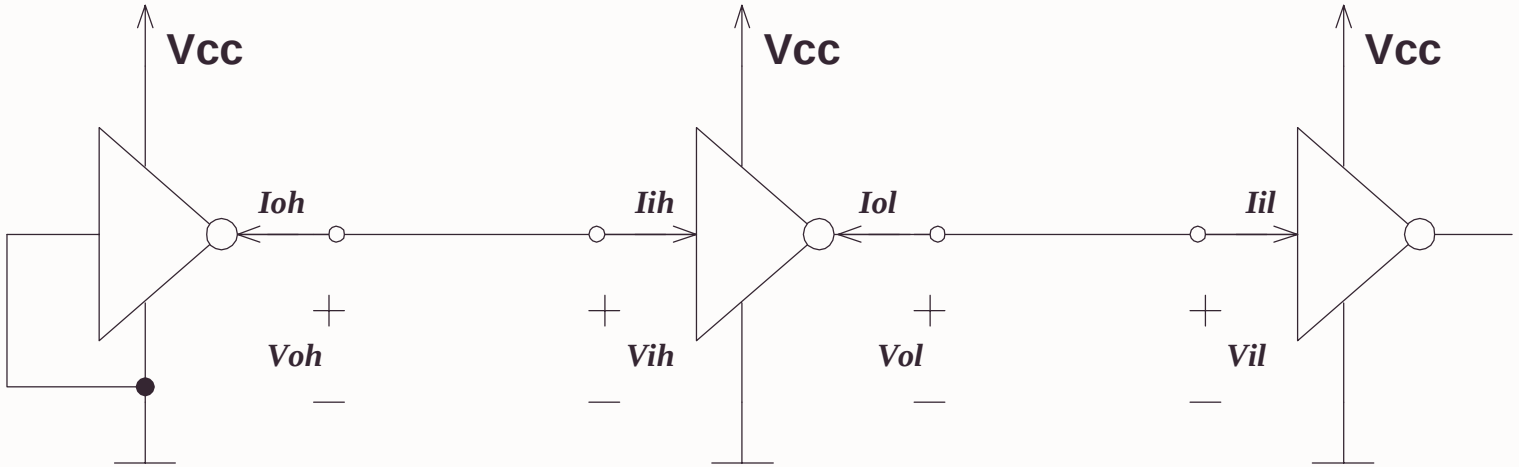
Source: G. Sery, Intel

Logic Families/Static VI Parameters



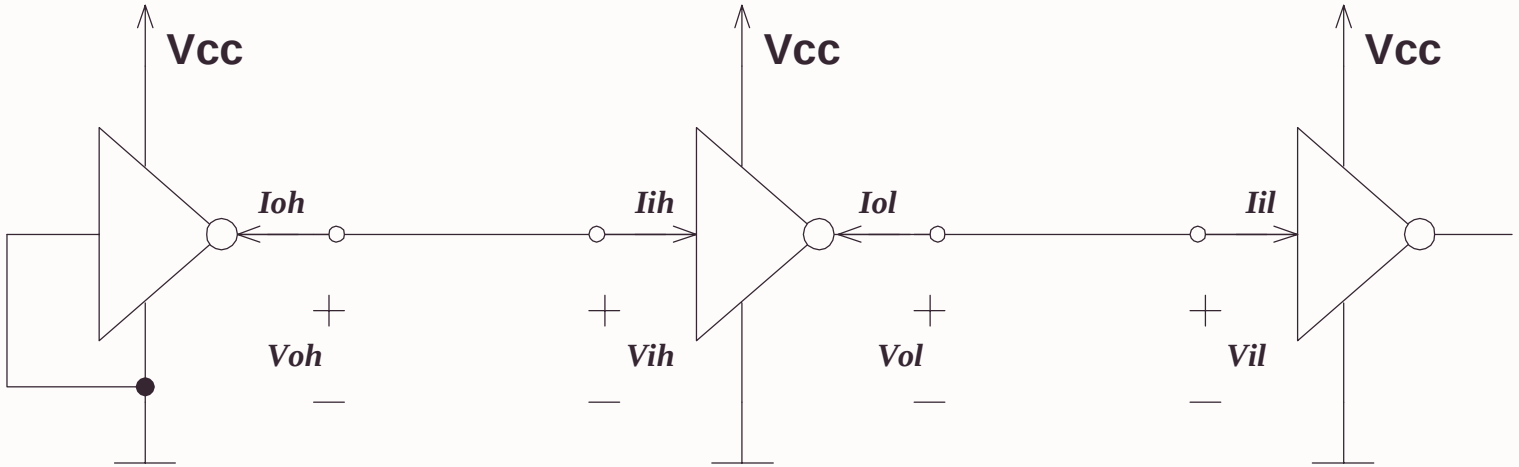
Parameter	Comment
Voh(min)	**High-Level Output Voltage**. The minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.
Vol(max)	**Low-Level Output Voltage**. The maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

Logic Families/Static VI Parameters



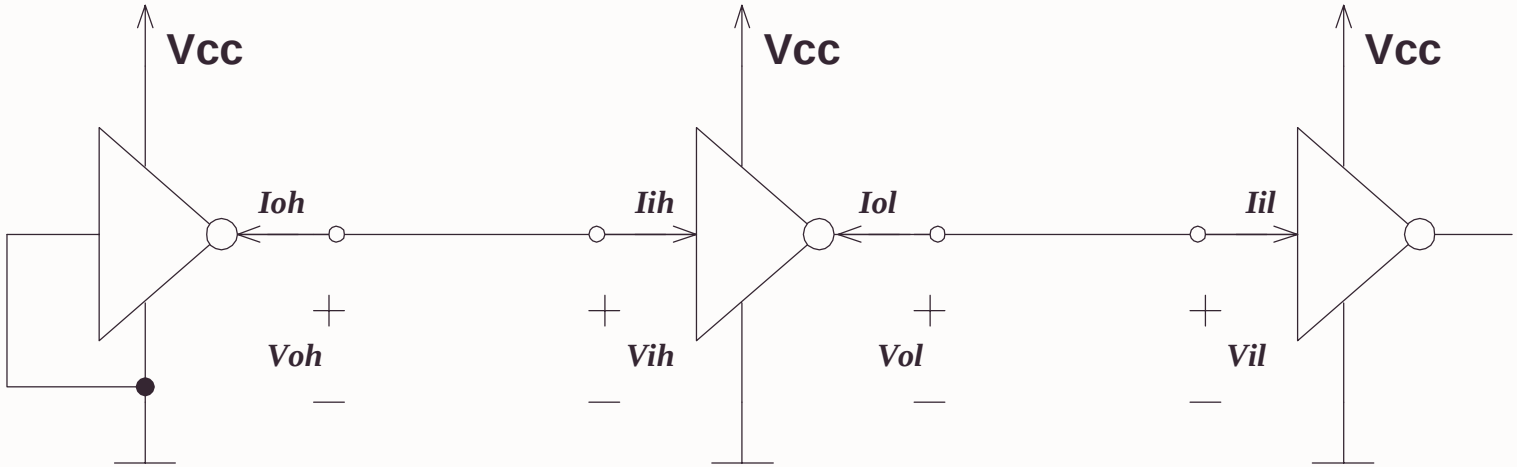
Parameter	Comment
Vih(min)	**High-Level Input Voltage**. The minimum voltage level required for a logical 1 at an input. Any voltage below this level may not be recognized as a logical 1 by the logic circuit.
Vil(max)	**Low-Level Input Voltage**. The maximum voltage level required for a logical 0 at an input. Any voltage above this level may not be recognized as a logical 0 by the logic circuit.

Logic Families/Static VI Parameters



Parameter	Comment
Ioh	**High-Level Output Current**. Current flowing into an output in the logical 1 state under specified load conditions.
Iol	**Low-Level Output Current**. Current flowing into an output in the logical 0 state under specified load conditions.

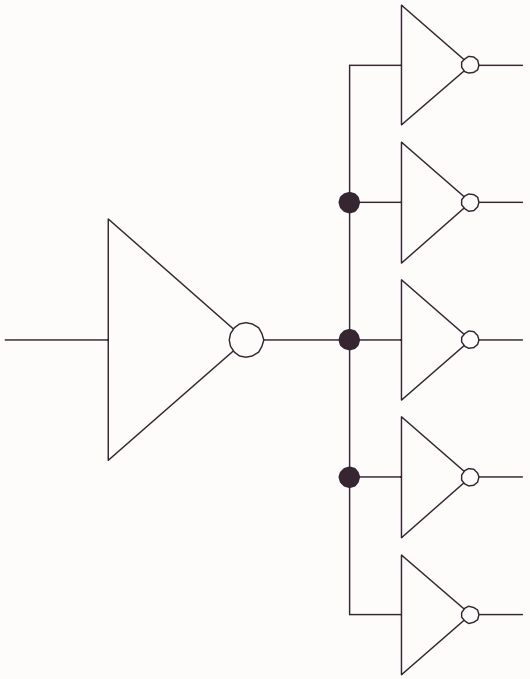
Logic Families/Static VI Parameters



Parameter	Comment
Iih	**High-Level Input Current**. Current flowing into an input when a specified high-level voltage is applied to that input.
Iil	**Low-Level Input Current**. Current flowing into an input when a specified low-level voltage is applied to that input.

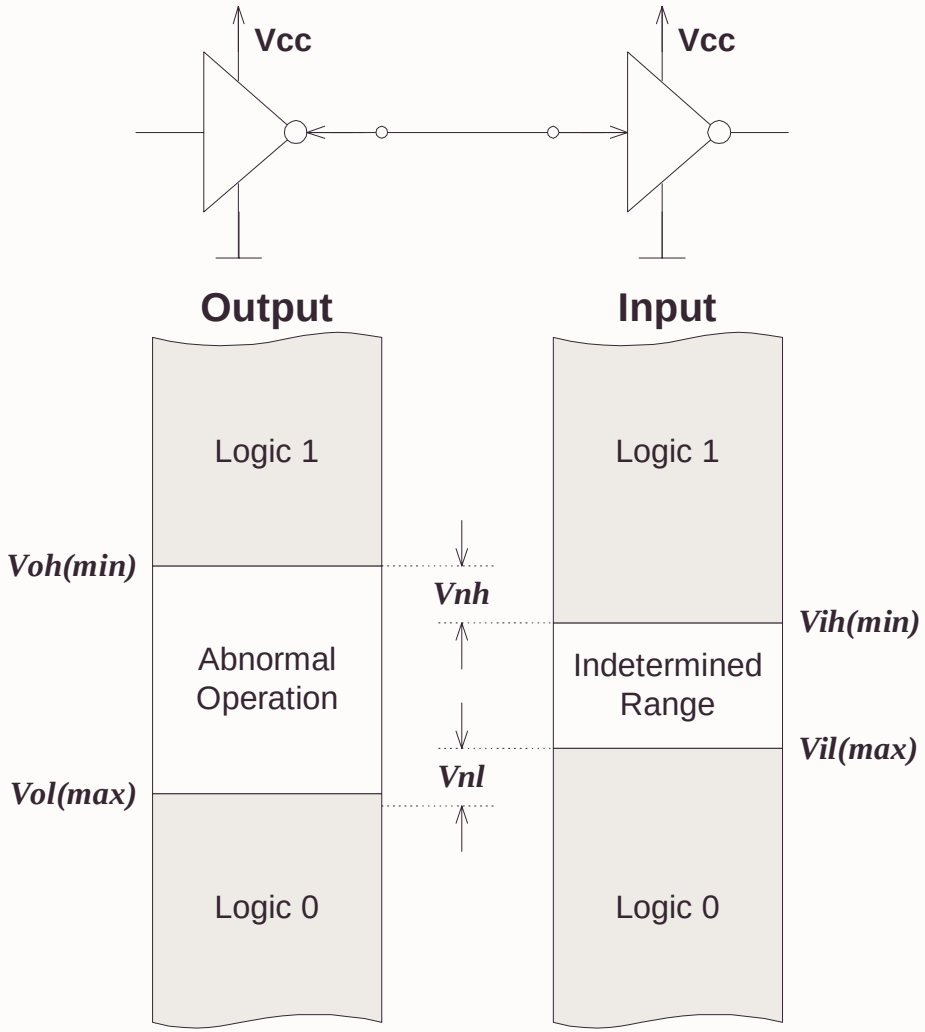
Logic Families/Fan-Out

– Fan-out: The maximum number of logic inputs that an output can drive reliably.



Beware:
Modern mixed-technology digital systems often employ logic from different logic families. In this case Fan-out is meaningless, unless the operating condition is specified exactly.
Unless otherwise specified, fan-out is always assumed to refer to ***load devices of the same family*** as the driving output.

Logic Families/Noise (Voltage) Margin



High state noise margin :

$$Vnh = Voh(min) - Vih(min)$$

Low state noise margin :

$$Vnl = Vil(max) - Vol(max)$$

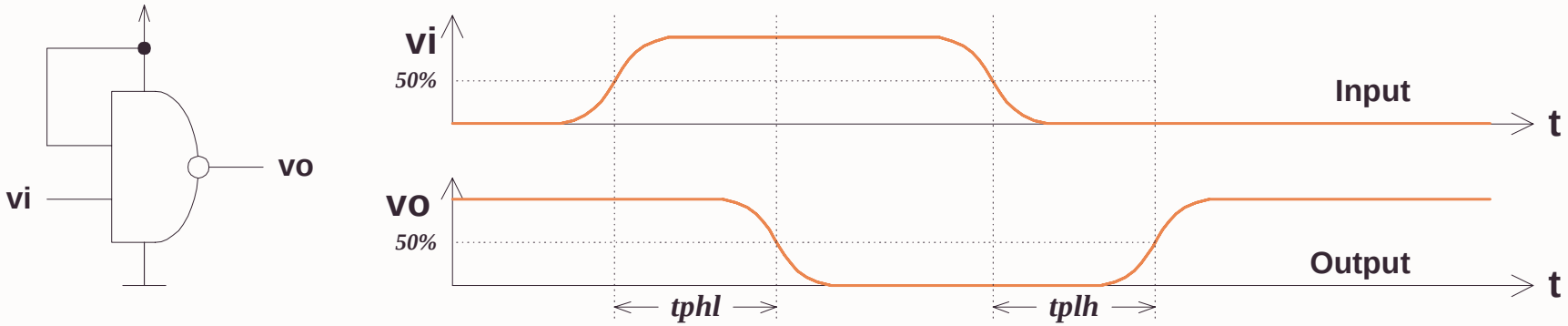
Noise margin :

$$Vn = min(Vnh, Vnl)$$

Noise margin required for reliable operation of digital systems in the presence of noise, crosscoupling, and ground-bounce.

Sometimes quoted: Percentage noise margin… bears little practical value.

Logic Families/Propagation Delay



Parameter	Comment
tphl	**Input-to-output propagation delay time** for output going from high to low.
tplh	**Input-to-output propagation delay time** for output going from low to high.

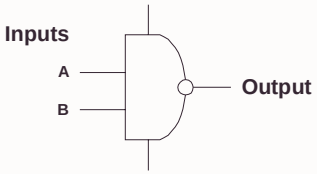
(Vague) comparison between logic families:

(e.g. for 74HC00: 25ns*100µW=2.5pJ)

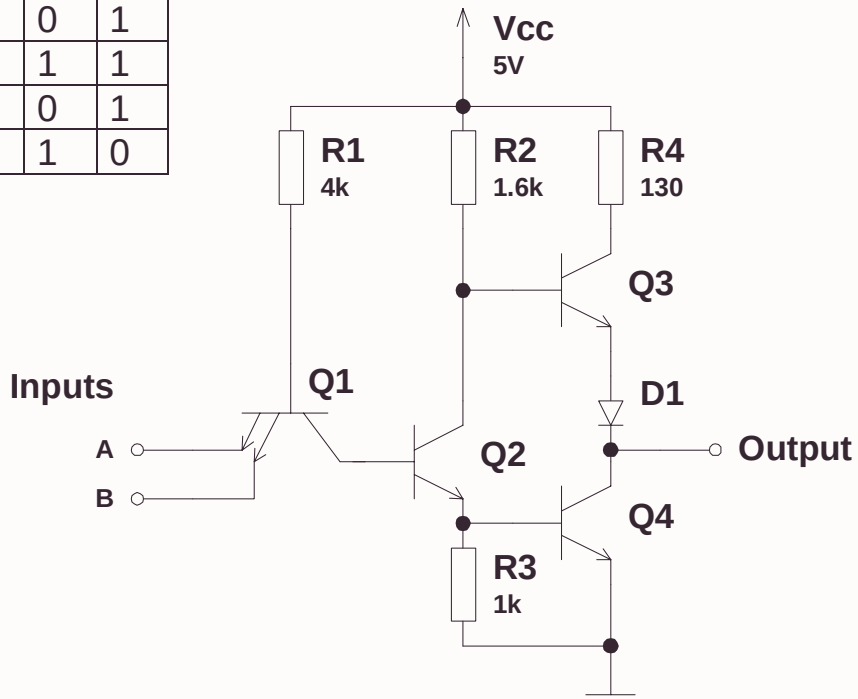
Gate Speed Power Product :

$$tp_{avg} \cdot Pdiss_{avg}$$

Logic Families/TTL Logic



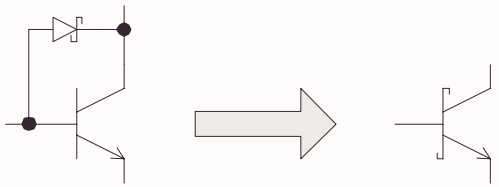
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



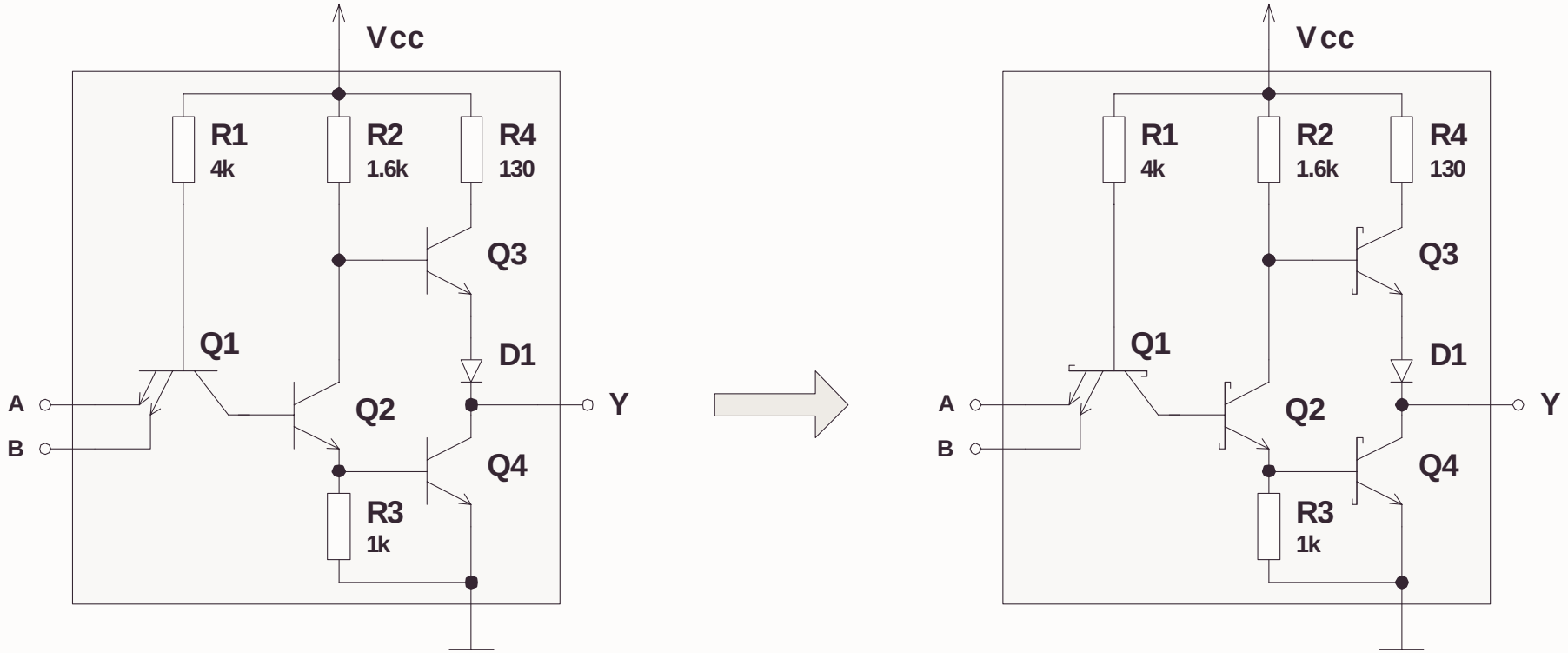
Standard TTL Logic:

- Bipolar Transistor-Transistor Logic
- Introduced in 1964 (Texas Instruments)
- Tremendous influence on the characteristics of all logic devices today
- Standard TTL shaped digital technology
- Standard TTL Logic (e.g. 7400) practically obsolete (i.e. replaced by more advanced logic families, e.g. 74ALS00)
- A large variety of logic functions available
- Single- or multi-emitter input transistor Q1 (up to eight emitters)
- Totem-pole output arrangement (Q3, Q4)

Logic Families/TTL/Logic Evolution



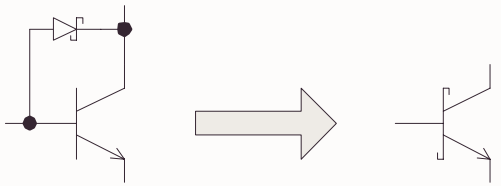
BJT (Bipolar Junction Transistor) storage time reduction by using a BC Schottky diode.
Schottky diode has a Vfw=0.25V. When BC junction becomes forward biased Schottky diode will bypass base current.



Logic Families/TTL/Logic Evolution

74 Series

Bipolar. Saturated BJTs. Practically obsolete. Don't use in new designs!



74S Series

Bipolar. Deep saturation prevented by BC Schottky Diode. Reduced storage-time delay. Practically obsolete.

74AS Series

Innovations in IC design and fabrication. Improvement in speed and power dissipation. Relatively popular. Fastest TTL available.

74LS Series

Bipolar. Lower-power slower-speed version of the 74S Series.

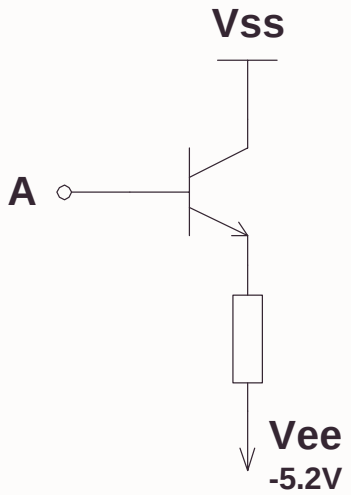
74ALS Series

Innovations in IC design and fabrication. Improvement in speed and power dissipation. Popular.

74F Series

Innovations in IC design and fabrication. Popular.

Logic Families/ECL



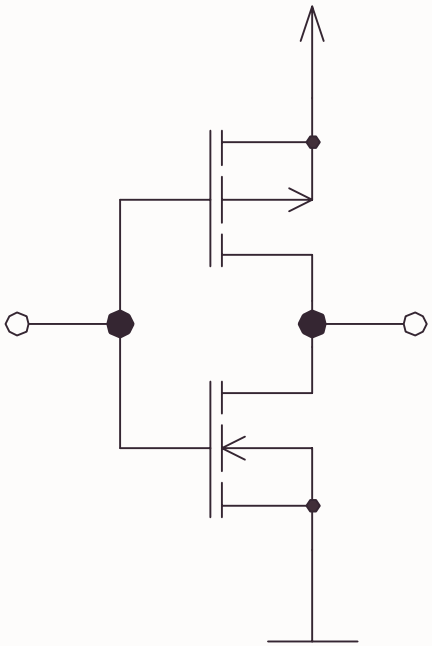
TTL
•BJTs operating in saturated mode
•Limited switching speed (storage time)

ECL (Emitter-Coupled Logic)
•BJTs operating in unsaturated mode (i.e. emitter-follower mode)
•Principle: Current switching (ECL is also sometimes called Current-Mode-Logic CML)

Advantages of ECL
•fastest logic family available

Disadvantages of ECL
•negative supply (awkward)
•high static power dissipation
•limited choice of manufacturers and devices
•low noise margin

Logic Families/CMOS



First CMOS logic family CD4000 introduced in 1968.

Because of their advantages CMOS devices have become dominant in the IC market

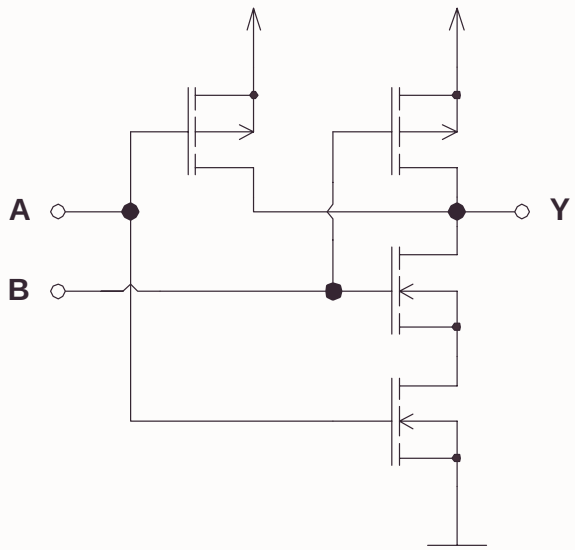
MOS Logic:
MOS: Metal-Oxide-Semiconductor (Metal-Oxide-Silicon

MOS Logic Categories:
•NMOS (obsolete)
•PMOS (obsolete)
•CMOS: complementary MOS

Advantages of MOS
•inexpensive and simple to fabricate
•high speed
•low static power consumption
•scaling of mosfets: higher integration possible
•rail-to-rail outputs

Disadvantages of MOS
•susceptibility to electro-static damage, ESD
•susceptibility to latch-up

Logic Families/CMOS



CMOS Gate Characteristics:

- No resistive elements (resistors elements require large chip areas in bipolar ICs)
- Extremely low static power consumption (Roff > $10^{10}\Omega$)
- Extremely low static input currents
- Cross-conduction and charge/discharge of internal capacitances lead to dynamic power dissipation
- Output Y swings rail-to-rail (low Ron)
- Supply voltage can be reduced to 1V and below

DO NOT leave CMOS inputs floating !
Unused CMOS inputs must be tied to a fixed voltage level (or to another input).

Logic Families/CMOS/Logic Evolution

4000 Series

CMOS. Wide supply voltage range. High noise margin. Low speed. Weak output drive. Practically obsolete.

↓

74C Series

CMOS. Pin-compatible with TTL devices. Low speed. Obsolete. Replaced by HC/HCT family.

↓

74HC/HCT Series

CMOS. Drastic increase in speed. Higher output drive capability. HCT input voltage levels compatible with TTL.

↓

74AC/ACT Series

CMOS. Functionally compatible, but not pin-compatible to TTL. Improved noise immunity and speed. ACT inputs are TTL compatible.

↘

74AHC/AHCT Series

CMOS. Improved speed, lower power, lower drive capability.

↘

BiCMOS Logic

CMOS/Bipolar. Combine the best features of CMOS and bipolar. Low power high speed. Bus interfacing applications (74BCT, 74ABT)

↘

74LVC/ALVC/LV/AVC

CMOS. Reduced supply voltage.
LVC: 5V/3.3V translation
ALVC: Fast 3.3V only
AVC: Optimised for 2.5V, down to 1.2V

CMOS Logic Trend:

Reduction of dynamic losses (cross-conduction, capacitive charge/discharge cycles) by decreasing supply voltages
(12V→5V → 3.3V → 2.5V → 1.8V → 1.5V…).

Reduction of IC power dissipation is the key to:

- lower cost (packaging)
- higher integration
- improved reliability

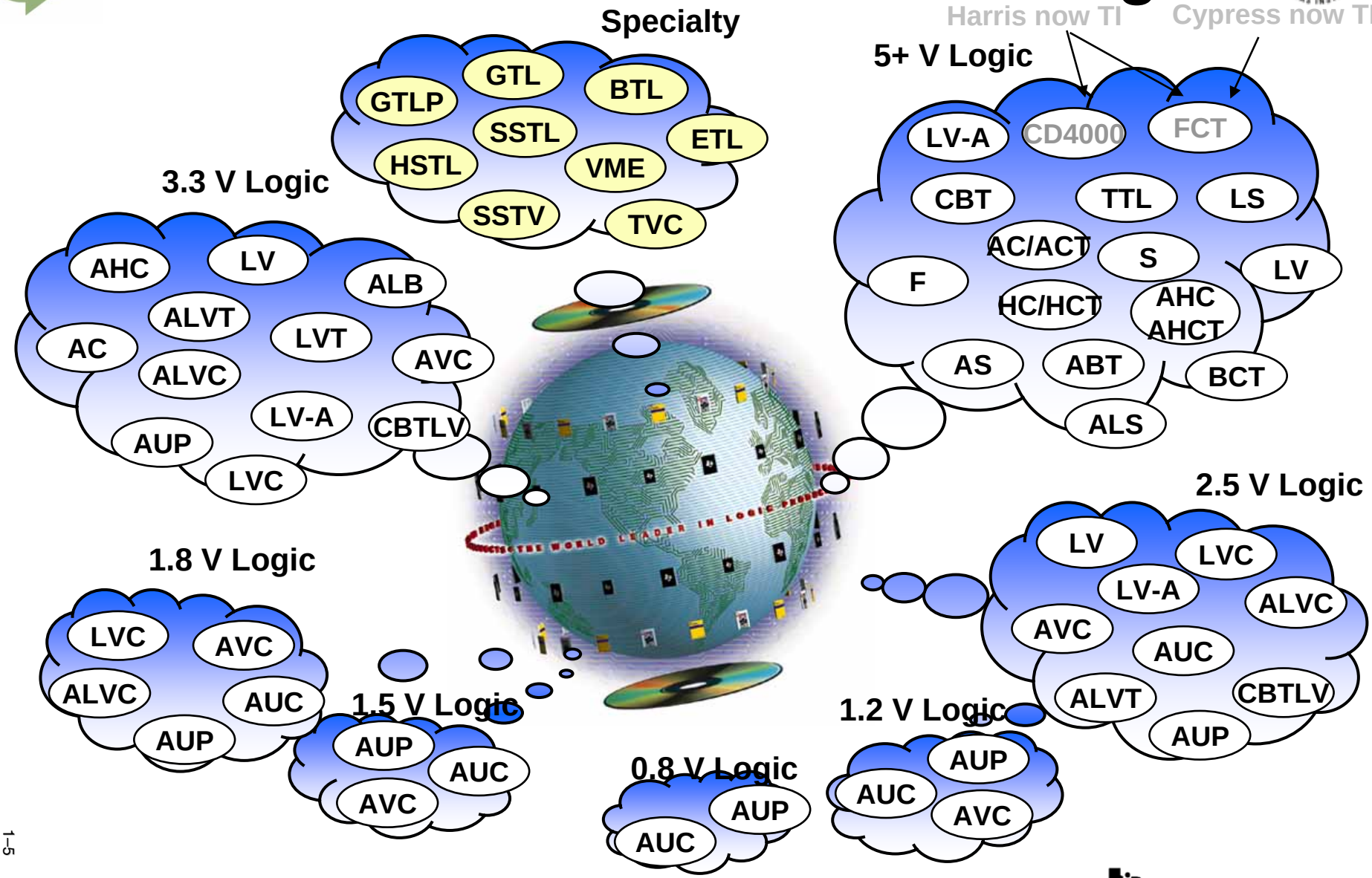
Logic Families/Overview

Logic Family	Prop. Delay	Rise/Fall Time	Vih_{min}	Vil_{max}	Voh_{min}	Vol_{max}	Noise Margin
74	22ns		2.0V	0.8V	2.4V	0.4V	0.4V
74LS	15ns		2.0V	0.8V	2.7V	0.5V	0.3V
74F	5ns	2.3ns	2.0V	0.8V	2.7V	0.5V	0.3V
74AS	4.5ns	1.5ns	2.0V	0.8V	2.7V	0.5V	0.3V
74ALS	11ns	2.3ns	2.0V	0.8V	2.5V	0.5V	0.3V
ECL	1.45ns	0.35ns	-1.165V	-1.475V	-1.025V	-1.610V	0.135V
4000	250ns	90ns	3.5V	1.5V	4.95V	0.05V	1.45V
74C	90ns		3.5V	1.5V	4.5V	0.5V	1V
74HC	18ns	3.6ns	3.5V	1.0V	4.9V	0.1V	0.9V
74HCT	23ns	3.9ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AC	9ns	1.5ns	3.5V	1.5V	4.9V	0.1V	1.4V
74ACT	9ns	1.5ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AHC	3.7ns		3.85V	1.65V	4.4V	0.44V	0.55V

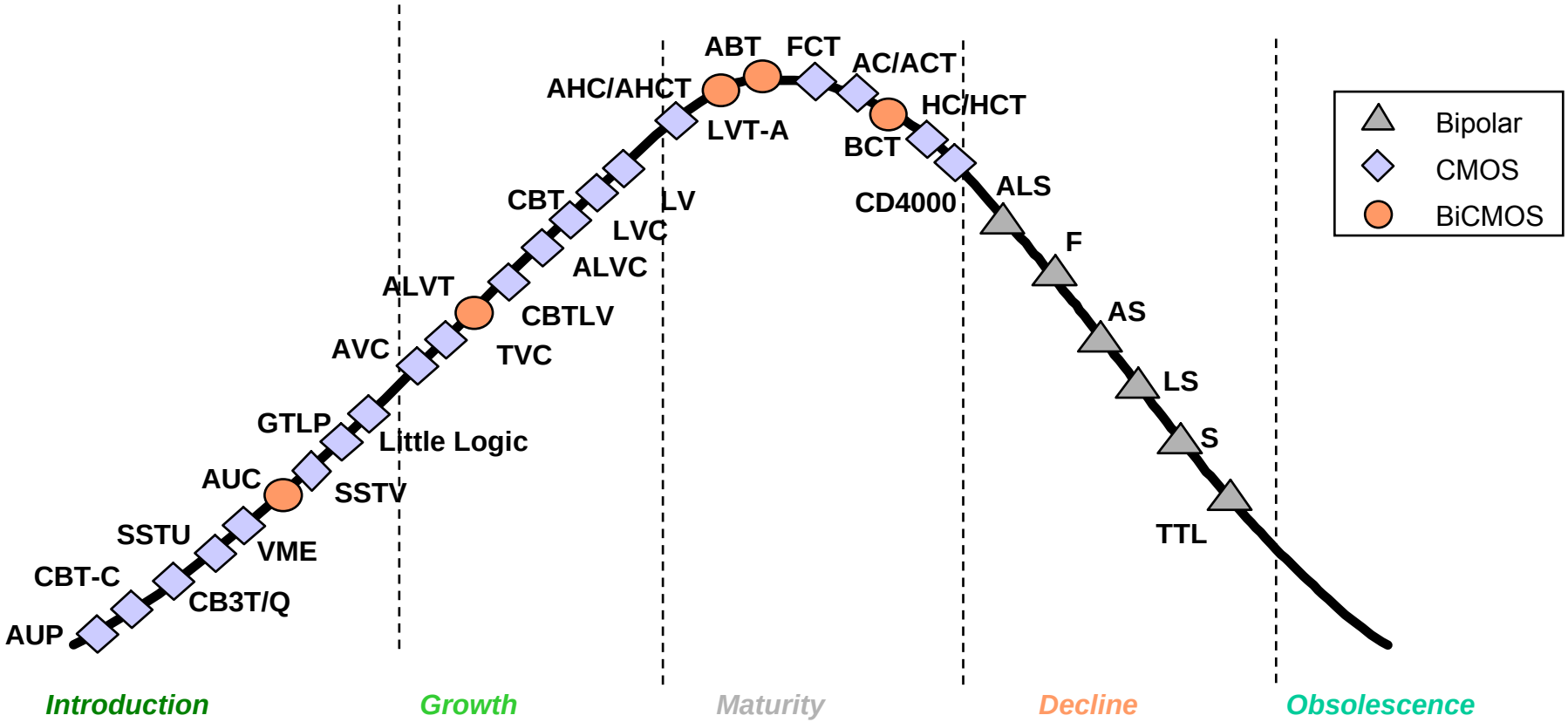
(Typical values for rough comparison only. Refer to datasheet. Values valid for Vcc=5V)

Care is needed when driving inputs of one logic family by outputs of a different family !
Watch voltage levels and fan-out !

Welcome to the World of TI Logic

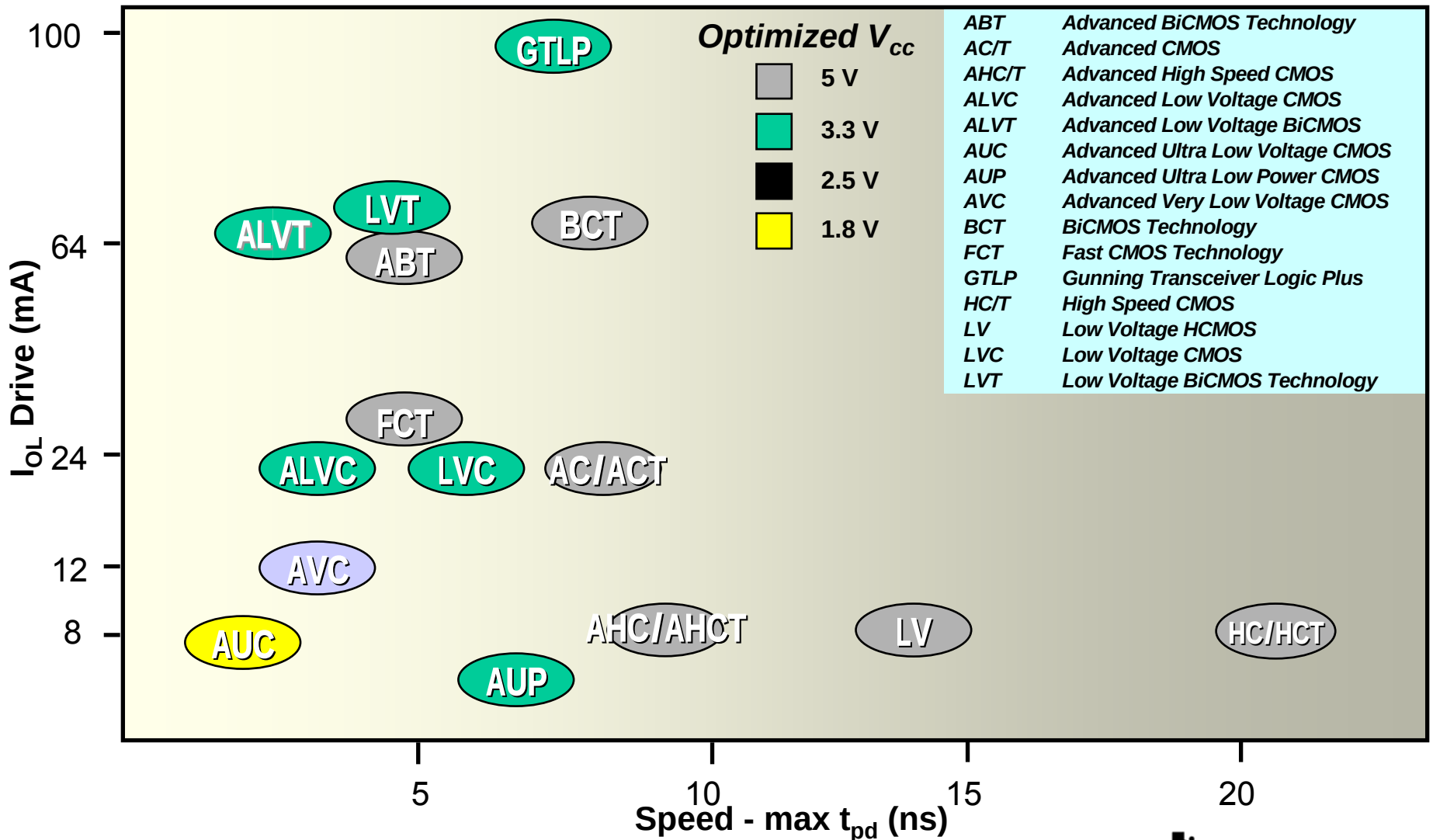


Product Life Cycle



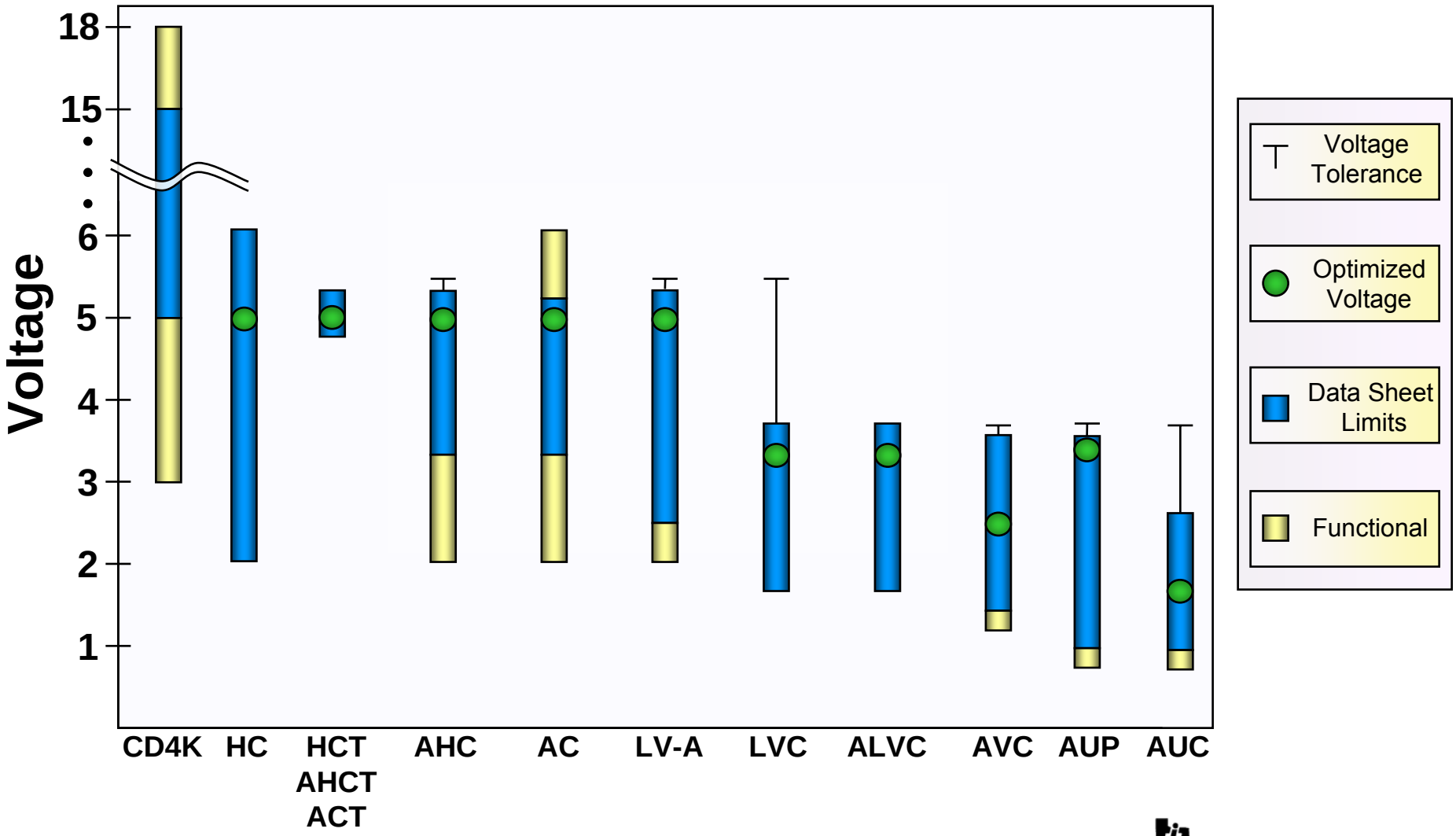
TI remains committed to be the last supplier in the older families.

Family Performance Positioning

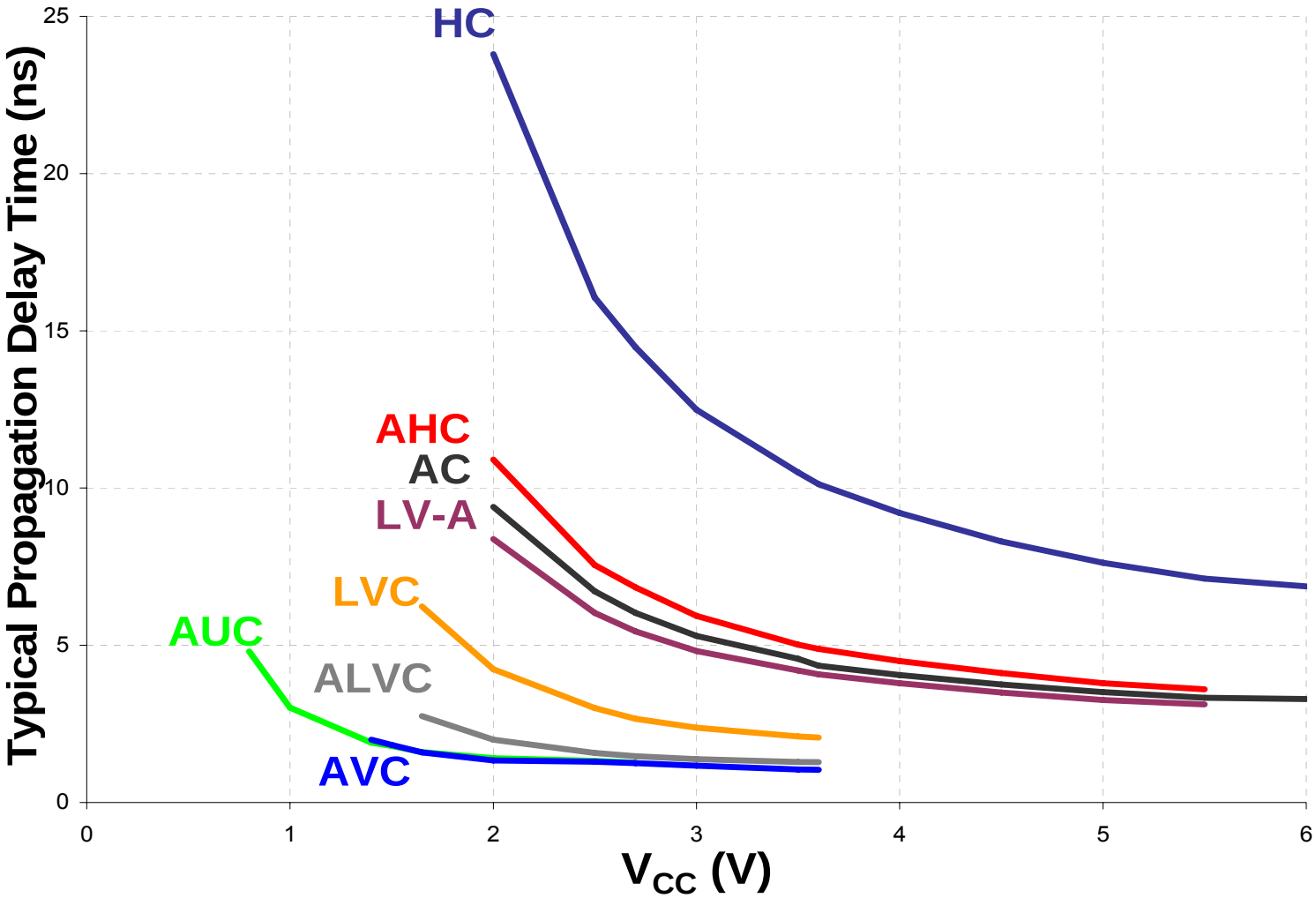


ABT	Advanced BiCMOS Technology
AC/T	Advanced CMOS
AHC/T	Advanced High Speed CMOS
ALVC	Advanced Low Voltage CMOS
ALVT	Advanced Low Voltage BiCMOS
AUC	Advanced Ultra Low Voltage CMOS
AUP	Advanced Ultra Low Power CMOS
AVC	Advanced Very Low Voltage CMOS
BCT	BiCMOS Technology
FCT	Fast CMOS Technology
GTLP	Gunning Transceiver Logic Plus
HC/T	High Speed CMOS
LV	Low Voltage HCMOS
LVC	Low Voltage CMOS
LVT	Low Voltage BiCMOS Technology

CMOS Voltage Roadmap



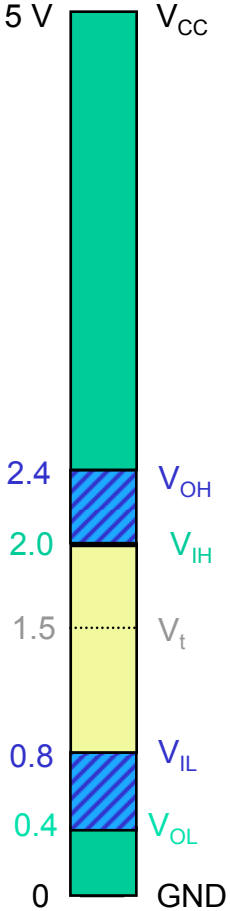
CMOS Voltage vs. Speed



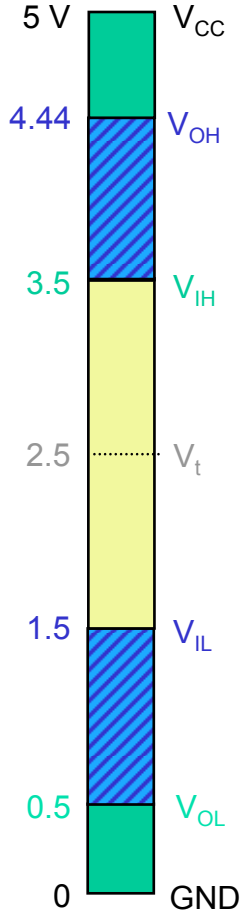
Comparison of 16245 functions with 500 ohm/30pF load. (AUC not yet tested)

IC Basics

Comparison of Switching Standards

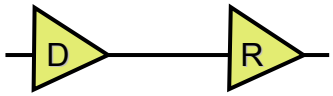


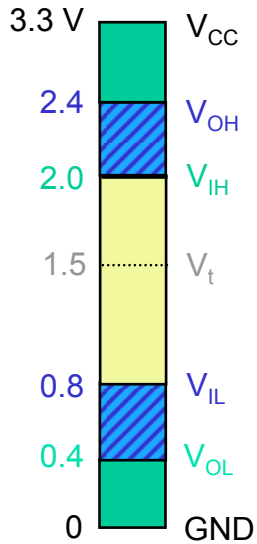
5-V TTL
Standard TTL: ABT, AHCT, HCT, ACT, Bipolar



5-V CMOS
Rail-to-Rail 5 V
HC, AHC, AC, LV-A

Is V_{OH} higher than V_{IH}?
Is V_{OL} less than V_{IL}?

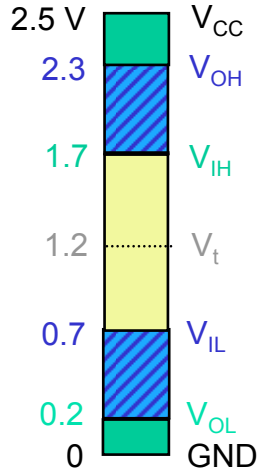




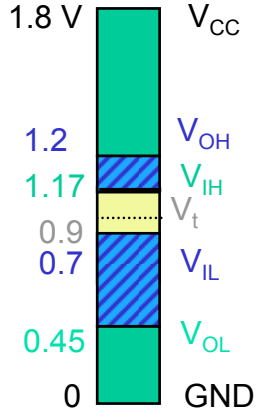
3.3-V LVTTL
LVT, LVC, ALVC
AUP, LV-A, ALVT

D \ R	5TTL	5CMOS	3LVTTL	2.5CMOS	1.8CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes

* Requires V_{IH} Tolerance



2.5-V CMOS
AUC, AUP, AVC,
ALVC, LVC, ALVT



1.8-V CMOS
AUC, AUP, AVC,
ALVC, LVC

TEXAS INSTRUMENTS

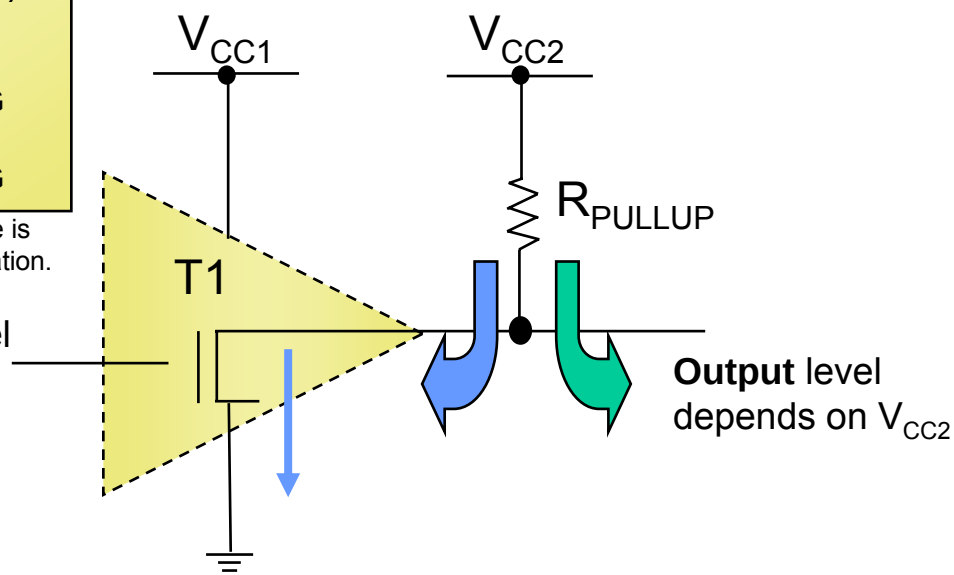
Mixed-Voltage Interfacing

Open-Drain Outputs 05/06/07 Functions

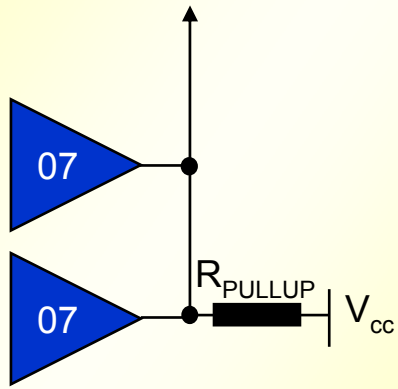
Functions Available

- 05 -S, LS, ALS, AC, HC, AHC, LV, LVC
- 06 -TTL, LS, LV, LVC, LVC1G/3G, AUC1G
- 07 -TTL, LS, LV, LVC, LVC1G/3G, AUC1G

NOTE: Over voltage tolerance is required to support UP translation.



Also Possible
Wired-Function Technique



Phantom links on output side can reduce component count.

Supply Voltage Vcc1	LV05A/06A/07A		LVC06A/07A		LVC1G07/2G07/3G07		Pullup resistor may be connected to	Level conversion range
	Vi Level	Speed	Vi Level	Speed	Vi Level	Speed		
1.8 V	NA	NA	1.8 V Levels	1- 3.5 ns	1.8 V Levels	2.4 - 8.3 ns	1.8V, 2.5V, 3.3V and 5V	1.8 V ⇨ 1.8V - 5.5V
2.5 V	2.5 V Levels	6.6 - 10.4 ns	2.5 V Levels	1 - 2.8 ns	2.5 V Levels	1 - 5.5 ns	1.8V, 2.5V, 3.3V and 5V	2.5 V ⇨ 1.8V - 5.5V
3.3 V	3.3 V Levels	5 - 7.1 ns	3.3 V Levels	1 - 2.9 ns	3.3 V Levels	1.5 - 4.2 ns	1.8V, 2.5V, 3.3V and 5V	3.3 V ⇨ 1.8V - 5.5V
5 V	5 V Levels	3.4 - 5.5 ns	5 V Levels	1 - 2.6 ns	5 V Levels	1 - 3.5 ns	1.8V, 2.5V, 3.3V and 5V	5 V ⇨ 1.8V - 5.5V

IC Packaging/Intro

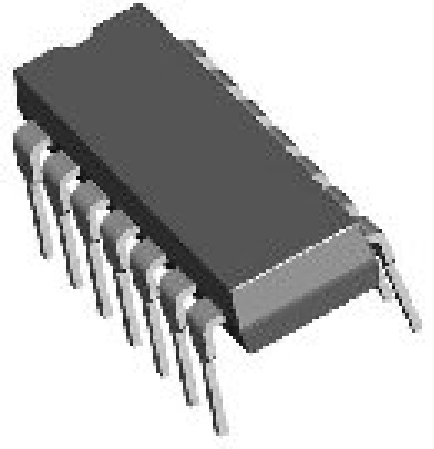
- ICs are at the core of a modern digital system
- Many systems fit entirely on a single IC (SOC)
  - a single $(15\text{-mm})^2$ chip can hold several million gates (1997)
  - a simple 32-bit CPU can be realised in an area of $1mm^2$
- Biggest limitation of a modern digital IC: Large reduction in signal count between on-chip wires and package pins. Typical IC
  - 10^4 wiring tracks on each of four metal layers
  - 10^3 signals can leave the chip (for cheaper packages: 40..200)
  - Chips are often “pad-limited”. Peripheral-bonded chips. Chip area increases as the square of the number of pads

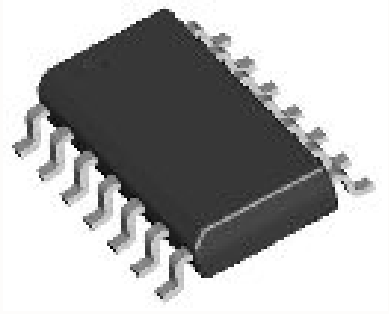
IC Packaging/Intro

- Most ICs are bonded to small IC packages
  Although it is possible to attach chips directly to boards. Method used extensively in low-cost consumer electronics. Placing chips in packages enables independent testing of packaged parts, and eases requirements on board pitch and P&P (pick-and-place) equipment.
- IC Packages
  - inexpensive plastic packages: <200 pins
  - packages with >1000 pins available
    (e.g. Xilinx FF1704: 1704-ball flip-chip BGA)
- IC Packaging Materials
  - Plastic, ceramic, laminates (fiberglass, epoxy resin), metal

IC Packaging/Categories

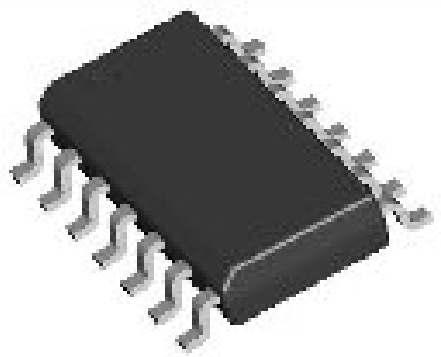
- IC package categories:
  - **PTH** (pin-through-hole)
    Pins are inserted into through-holes in the circuit board and soldered in place from the opposite side of the board
    - » Sockets available
    - » Manual P&P possible
  - **SMT** (surface-mount-technology)
    SMT packages have leads that are soldered directly to corresponding exposed metal lands on the surface of the circuit board
    - » Elimination of holes
    - » Ease of manufacturing (high-speed P&P)
    - » Components on both sides of the PCB
    - » Smaller dimensions
    - » Improved package parasitic components
    - » Increased circuit-board wiring density





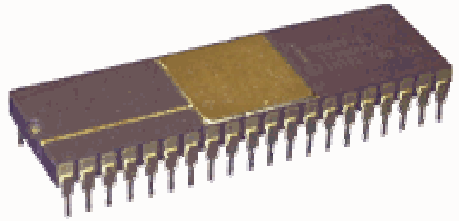
SMT packages offer many benefits and are generally preferred.

IC Packaging/Materials



- IC packaging material: Plastic
  - – die-bonding and wire-bonding the chip to a metal lead frame
  - – encapsulation in injection-molded plastic
  - – inexpensive but high thermal resistance
  - – **Warning**: Plastic molds are hygroscopic
    - » Absorb moisture
      Storage in low-humidity environment. Observation of factory floor-life
    - » Stored moisture can vapourise during rapid heating
      can lead to hydrostatic pressure during reflow process. Consequences can be: Delamination within the package, and package cracking. Early device failure.

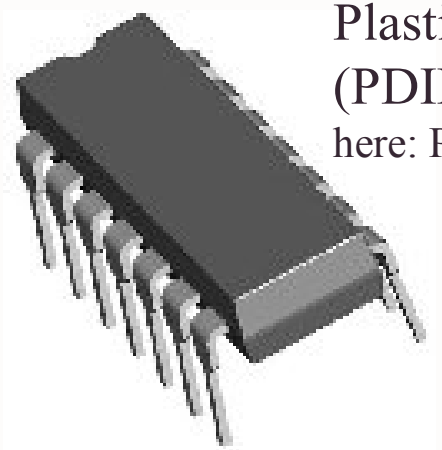
IC Packaging/Materials



- IC packaging materials: Ceramic
  - » consists of several layers of conductors separated by layers of ceramic (Al_2O_3 "Alumina")
  - » chip placed in a cavity and bonded to the conductors
    Note: no lead-frame
  - » metal lid soldered on to the package
  - » sealed against the environment
  - » ground layers and direct bypass capacitors possible within a ceramic package
  - » high permittivity of alumina ($\varepsilon r=10$)
    Note: High permittivity leads to higher propagation delay!
  - » expensive

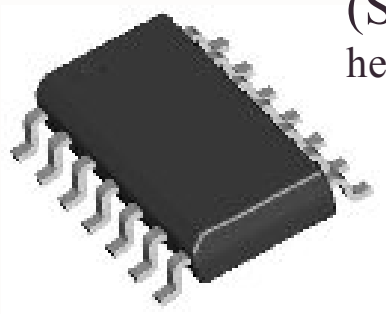
IC Packaging/Popular IC Packages

Plastic Dual-In-Line (PDIP)
here: PDIP14

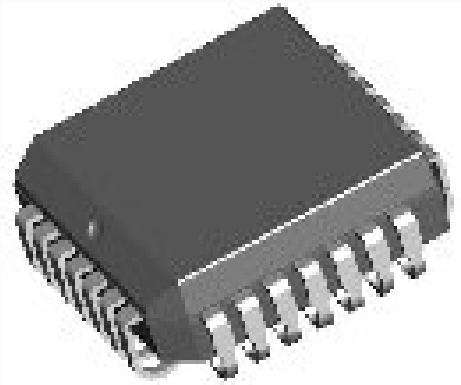


SC70
here: SC70-5

Small Outline Integrated Circuit (SOIC)
here: SO14



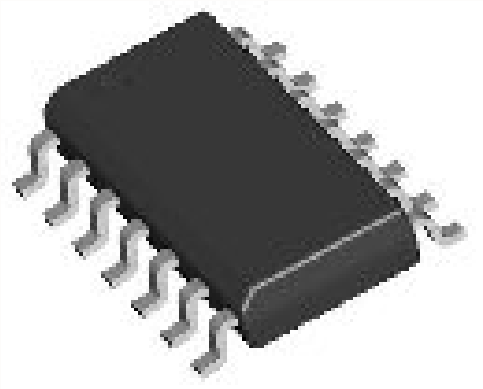
Plastic Lead Chip Carrier (PLCC)
here: PLCC28



Thin Shrink Small Outline (TSSOP)
here: TSSOP14

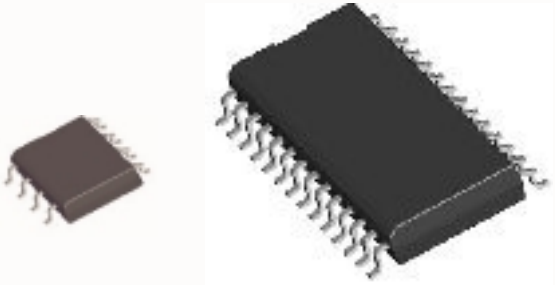
Thin Quad Flat Package (TQFP)
here: TQFP32

IC Packaging/Popular IC Packages

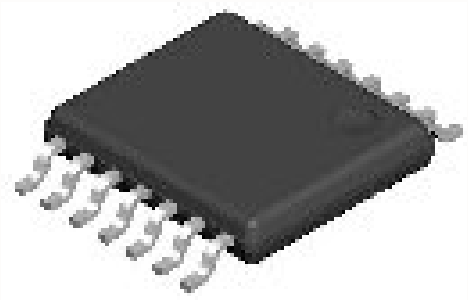


Small Outline Integrated Circuit (SOIC)

- Shown: SO14, but available from SO8..SO28
- Gull-wing leads
- Popular, cost effective, and widely available IC package for low-pin-count ICs
- Dimensions: 8.6mm x 3.9mm x 1.75mm
- Pin-to-pin: 1.27mm (50mil)

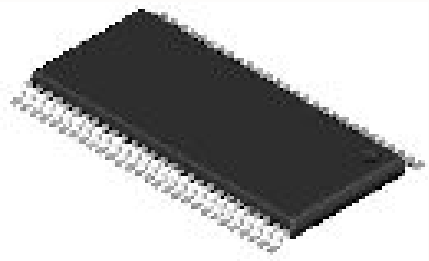


IC Packaging/Popular IC Packages



Thin Shrink Small Outline (TSSOP)

- Shown: TSSOP14, but available up to TSSOP64
- Popular, cost effective, and widely available IC package for low-profile applications
- Dimensions: 5.0mm x 4.4mm x 1.2mm
- Pin-to-pin: 0.65mm (25mil)



IC Packaging/Popular IC Packages

Ball Grid Arrays (BGA)

- Shown: BGA54
- Available pin count >1700
- Advanced IC package for high-density low-profile applications
- Chip-scale package (CSP)
- Dimensions: 8.0mm x 5.5mm x 1.4mm
- Pin-to-pin: 0.8mm
- Low lead inductance

Altera Ultra-Fine-Line BGA

- Pin-Count: 169
- Dimensions 11mm x 11mm
- Profile: 1.2mm

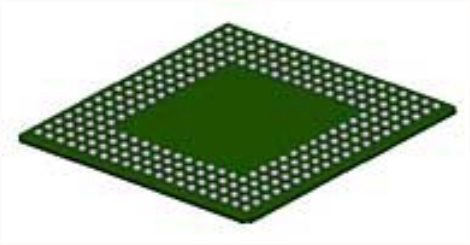
Challenges:

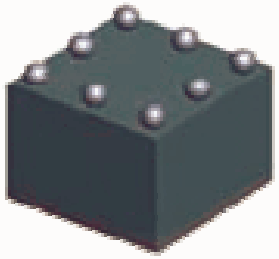
- **Integrity of solder joints**
- **Solder joint inspection (X-ray)**
- **Availability of 2nd source**
- **Routing**

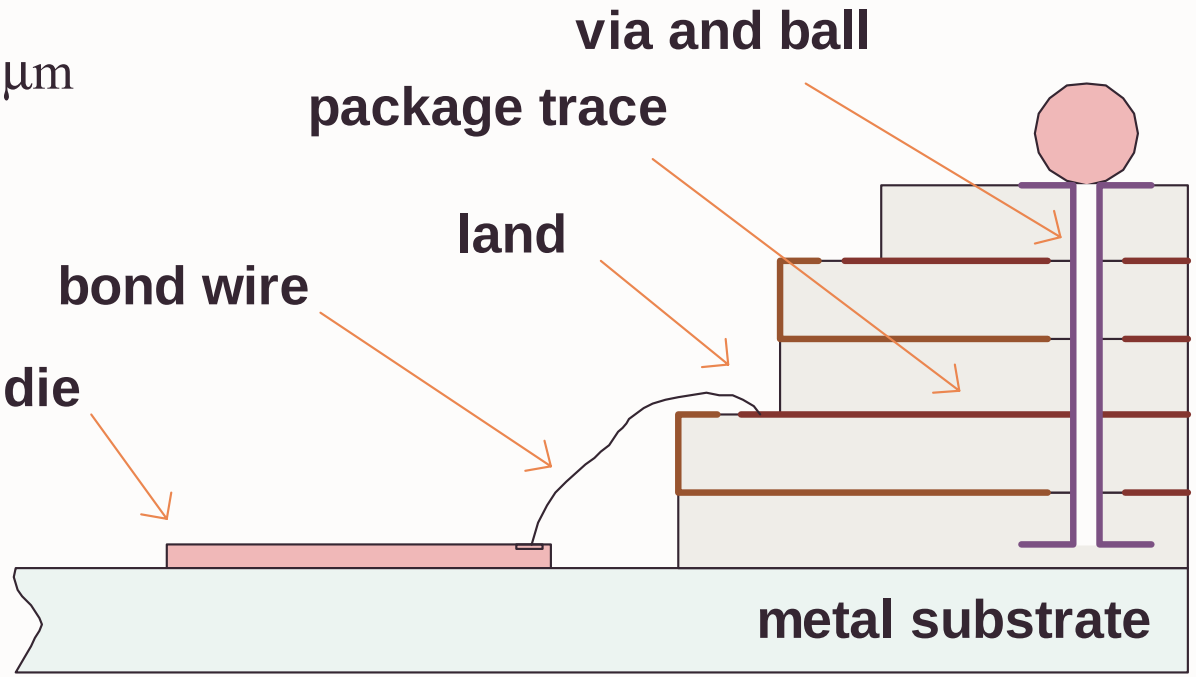
IC Packaging/BGA Physical Construction

Physical construction of a BGA

- Shown: Type-II BGA (cavity-down design)
- Interconnect: multi-layer laminated construction
- Die bonded onto a metal heat slug
- Solder balls make connection to a PC board
- 50µm bond wires
- Copper conductor thickness 20µm
- Layer separation 150µm





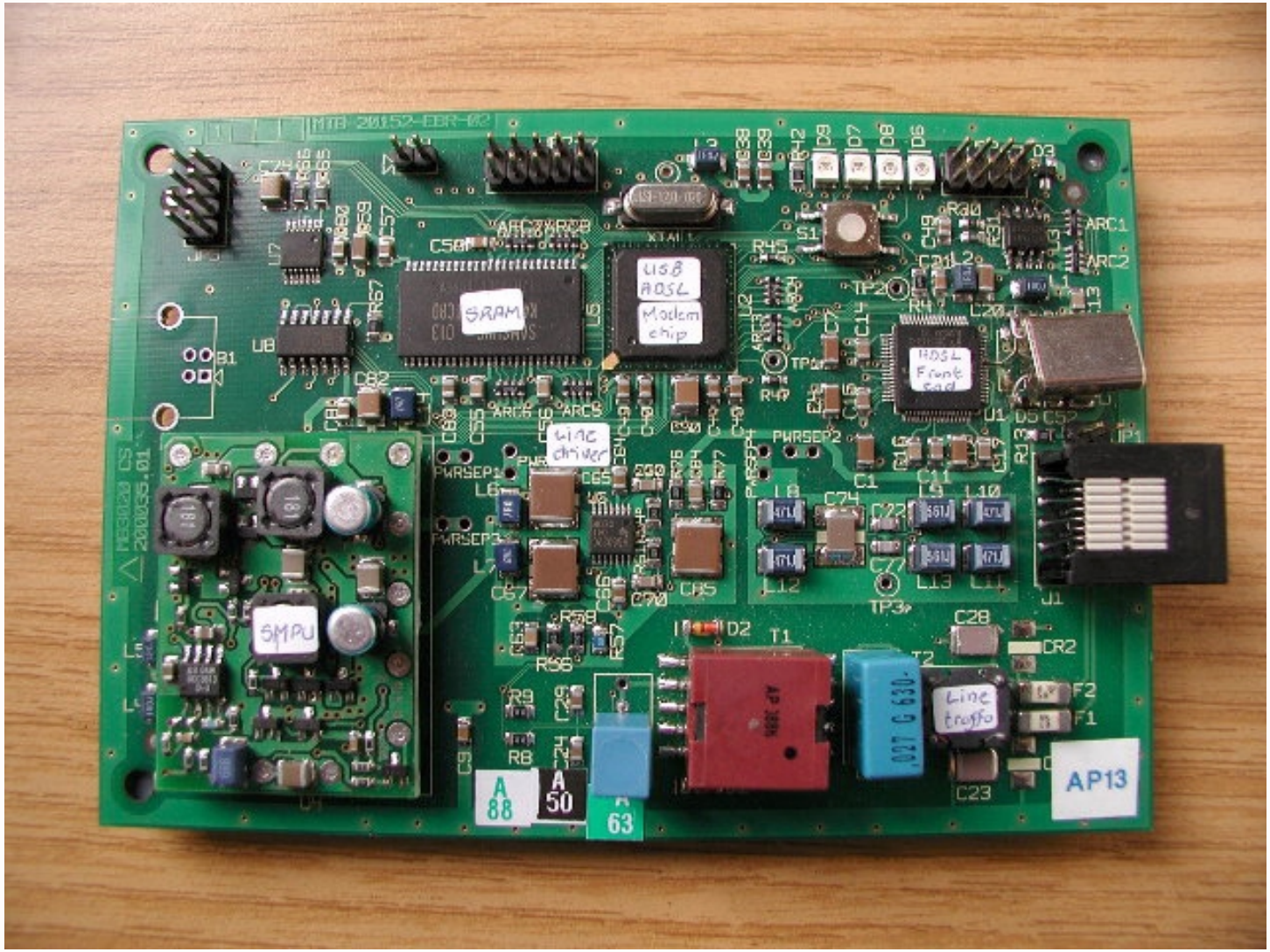


IC Packaging/Electronic Assembly (1981)

IBM PC 1981

- IC packaging: DIL only!
- Processor: 8088
- Memory: 256kB

IC Packaging/Electronic Assembly (2000)



Low-density electronic assembly with various IC packages

- SO
- TSSOP
- QFP
- BGA