# **4A** 1

### Lecture 4A – Diode Circuits

The peak detector. The clamp circuit. The clipping circuit.

#### **The Peak Detector**

Consider the following circuit:





The state of the diode will affect the analysis of the circuit. Since there are only two ways in which an ideal diode can operate ("on" or "off"), we will assume that the diode is in some state initially. Once a diode is assumed to be "on" or analysis cannot be "off", an analysis of the circuit can be carried out.

Normal circuit used with diodes

After the analysis, we will check our original assumption to see that it is valid. If it is, then the analysis is complete, otherwise we assume the opposite state for the diode, and carry out another analysis. For example, after assuming the diode to be "on", we may find that the current in the diode goes from cathode to anode - which is impossible. The initial assumption of the diode being "on" must therefore be wrong. We should start the analysis again, but this time assume that the diode is "off".

Circuit analysis starts with an assumption - which is later checked

In analysing circuits with diodes, we will always initially assume that a diode is We always assume in the "off" state. After carrying out an analysis, we should check that the diode initially "off" is indeed in the "off" state. This condition corresponds to the diode being reverse biased. In other words, the diode voltage,  $v_d$ , should be negative. If it is not, then the diode is really "on", and we have to repeat the analysis.

that diodes are



Let's first look at an isolated capacitor subjected to a sinusoidal voltage:



We know for a capacitor that:

$$q = Cv \tag{4A.1}$$

When a capacitor stores charge, it has positive charge on one plate, and negative on the other. An electric field therefore exists between the plates of the capacitor. To move a positive charge from the negative plate to the positive plate through the electric field means doing work. The voltage across a capacitor is the work done per unit charge in doing this. For each voltage, there corresponds a unique proportional charge. The proportionality constant is called the capacitance.

Initially the capacitor holds no charge, so the voltage across it is zero. (This doesn't mean it is a short circuit, it just means there is no electric field to oppose moving a charge from one plate to the other).

When the voltage across the capacitor is increased, the charge increases in proportion. We are "putting positive charge onto the positive plate, and removing it from the negative plate". With the sign convention as in Figure 4A.2, this implies a positive current.

If the voltage across a capacitor is not changing, then the charge it is storing cannot be changing either. Therefore, the current must be zero.

Storing charge in a capacitor produces a voltage

The current and voltage relationship in a capacitor

If there is no stored charge in a capacitor, there is no voltage

When we decrease the voltage across a capacitor, we have to decrease the amount of stored charge. This means we must "remove positive charge from the positive plate, and put it on the negative plate". This means negative current using our sign convention.

The above reasoning is summed up by differentiating Eq. (4A.1) with respect to time:

 $i = C \frac{dv}{dt}$ 

(4A.2)

The current "through" a capacitor depends only on the rate of change of voltage with respect to time

Now consider our peak detector circuit again. Notice that the output is taken across the capacitor, so it is this voltage that we are interested in. We will assume that the source is a sine wave (not a cosine wave). We also assume, as always, that the diode is "off" initially. This means there is no current in the circuit and KVL around the loop gives:

$$v_s - v_d - v_c = 0 \tag{4A.3}$$

But since there is no charge on the capacitor initially:

$$v_s - v_d = 0$$

$$v_d = v_s \tag{4A.4}$$

This means the source voltage appears directly across the diode. But the source voltage is a sine wave, and it is positive initially. We can never have a positive across an ideal voltage across an ideal diode - its characteristic does not allow it. We must wrong assumption have made a wrong assumption – the diode must initially be in the "on" state.

A positive voltage diode means a start again

With the diode "on", KVL gives:

$$v_s - R_s i_d - v_c = 0$$
  
$$v_c = v_s - R_s i_d$$
(4A.5)

If the source resistance is small, then we may say:

$$V_C \approx V_s$$
 (4A.6)

Therefore, initially, the output of the peak detector equals the input. The capacitor will have the same voltage as the source until it reaches its peak.

As soon as the source voltage tries to reduce the capacitor voltage, we know that the current in the capacitor must be negative (with respect to the defined current direction). Since the diode blocks current in this direction, there will be no current. After the capacitor voltage reaches the peak of the source voltage, the diode will not allow reverse current, and will be reverse biased when the source voltage decreases from its peak value.

If the diode is "off", then the capacitor cannot discharge, so its voltage will be:

$$v_C \approx \hat{v}_s$$
 (4A.7)

We analysed the circuit before when the diode was "off". In this case, Eq. (4A.3) gives for the diode reverse bias voltage:

$$v_d = v_s - v_C \approx v_s - \hat{v}_s \tag{4A.8}$$

From this equation, we can see that the diode voltage will always be negative or just on zero. The diode will therefore remain reverse biased for all time, so the capacitor will retain its voltage for all time.

A negative current through an ideal diode means a wrong assumption start again



A graph of the various voltages in the peak detector is shown below:

Figure 4A.3

The diode will not conduct again until the source voltage changes so as to exceed the capacitor voltage.

The steady-state output of the peak detector is obviously DC. What would happen if we try to use the peak detector as a DC voltage source? Consider the detector output following circuit, which is just a peak detector with a load resistor attached to the output:



Figure 4A.4

Assume there is no charge on the capacitor initially. The circuit will behave exactly as before, and the diode will be in the "off" state at the peak of the source voltage. With the diode "off" the circuit looks like:



Figure 4A.5

Writing KCL at the output node gives:

$$C\frac{dv_o}{dt} + \frac{v_o}{R} = 0 \tag{4A.9}$$

Rearranging and integrating with respect to time, we get:

$$\frac{1}{v_o} \frac{dv_o}{dt} = \frac{-1}{RC}$$

$$\int_0^t \frac{1}{v_o} \frac{dv_o}{dt} dt = \int_0^t \frac{-1}{RC} dt \qquad (4A.10)$$

A load on a peak detector output now provides a path for capacitor discharge current Performing the integral and rearranging, we get an expression for the voltage across the load:

$$\ln\left[\frac{v_o(t)}{v_o(0)}\right] = \frac{-t}{RC}$$
$$\frac{v_o(t)}{v_o(0)} = e^{-t/RC}$$
$$v_o(t) = v_o(0)e^{-t/RC}$$
$$v_o(t) = \hat{V_C}e^{-t/\tau}$$
(4A.11)

We have assumed (arbitrarily) that t = 0 is the instant the diode switches "off". Therefore, when the diode is "off", the voltage across the load experiences an experiences exponential decay. The *time constant*,  $\tau = RC$ , is determined by the capacitor and the resistor. The larger the value of capacitance and resistance, the slower the decay.

The output voltage exponential decay

The voltage will continue to decay until the input voltage has a higher value until the next than the load voltage, at which point the diode turns "on". This will charge the charging cycle capacitor up to the peak value of the input voltage again. A cycle will then be established.



A graph of the voltages and the source current is shown below:

Figure 4A.6

If the time constant  $\tau$  is large, then the exponential term in Eq. (4A.11) can be approximated by a linear term:

$$e^{x} = 1 + x + \frac{x^{2}}{2} + \frac{x^{3}}{3} + \dots$$
  

$$\approx 1 + x \quad \text{if } x \text{ is small}$$
  

$$v_{o}(t) \approx \hat{V}_{c} \left(1 - \frac{t}{RC}\right) \qquad (4A.12)$$

The output, when the diode is "off", therefore looks like a straight line.

Since the discharge time is much larger than the charging time, we can approximate the discharge time by the period of the source, T.

For slow exponential decay, a straight line is a good approximation

The peak-to-peak ripple (AC) and average (DC) parts of the voltage are then given by:

$$V_{r} = \hat{v}_{o} - \hat{v}_{o} \left(1 - T/RC\right)$$

$$= \frac{\hat{v}_{o}T}{RC} = \frac{\hat{v}_{o}}{fRC}$$

$$V_{DC} = \hat{v}_{o} - \frac{1}{2}V_{R}$$

$$= \hat{v}_{o} - \frac{\hat{v}_{o}}{2fRC}$$
(4A.13)

The approximate DC voltage produced by a loaded peak detector

To decrease the ripple we choose large values for R and C, and if we can, f.

To observe the ripple, we can pass the output voltage to a capacitively coupled load (e.g. a DSO on AC coupling).

#### **The Clamp Circuit**

Consider the following circuit:



Figure 4A.7

Assume initially the diode is off. The source voltage is assumed to rise from zero – it is a sine wave. In addition, assume that  $R_s$  is small and therefore  $v_i \approx v_s$ .

The diode will remain reverse biased until the source goes negative, since KVL around the loop gives:

 $\mathbf{\Omega}$ 

$$v_s + v_d = 0$$

$$v_d = -v_s \tag{4A.14}$$

(Remember initially that the voltage across the capacitor is 0 V - it holds no charge. Also, there is no voltage across the source resistance, since the diode is like an open circuit – there is no current).

Our assumption that the diode is off breaks down when the source voltage goes negative, since then a positive voltage exists across the diode. This condition must not happen, so our assumption is wrong. The diode must be forward biased and also conducting current when this occurs.

The current charges the capacitor, so that the voltage defined in Figure 4A.7 has a positive value. Doing KVL around the loop gives for the capacitor voltage:

$$v_C = -v_i \tag{4A.15}$$

(Remember that the diode is ideal, so it has no voltage drop across it when conducting. Also remember that at this stage the input voltage is negative, so that the capacitor voltage, as defined by the above equation, will be a positive number).

When the source reaches its negative peak, the current will reach zero. *Why?* At this point, the current would like to reverse direction. The source voltage is trying to decrease in *magnitude*, which means the charge stored on the capacitor will have to decrease. This can only be achieved by a current that draws positive charge off the positively charged plate – in effect, a current in the opposite direction to that shown in Figure 4A.7. This also corresponds to wanting a negative current in the capacitor, as explained previously. Since current cannot go in this direction – it is prevented by the diode – there will be

The diode prevents the capacitor from discharging no current and the diode may be considered off. With the diode off, the capacitor cannot discharge, and the voltage across it will be:

$$v_C = \hat{v}_i \tag{4A.16}$$

This is only true for a symmetric waveform. In general, the capacitor will charge to the magnitude of the negative peak of the waveform.

KVL around the loop then gives:

$$v_o = v_i + v_C = v_i + \hat{v}_i$$
 (4A.17)

The output is seen to be shifted by a DC voltage equal to the magnitude of the negative peak of the input voltage. The output voltage is said to have its lowest point *clamped* to zero – it cannot go below zero. The circuit is therefore known as a *positive clamp* circuit. Since the output is always positive, the diode is always reverse biased and will not conduct again. *Confirm this by doing KVL around the loop*.

The output voltage is a shifted version of the input voltage – it is alternating but unipolar

A graph of the various voltages is shown below:



Figure 4A.8

#### **The Clipping Circuit**

Consider the following circuit:





Figure 4A.9

The circuit works very simply. Assume both diodes are off. KVL then gives:

$$v_o = v_s \tag{4A.18}$$

If the output voltage is less than  $E_1$ , then diode  $D_1$  cannot be reversed bias, so it will conduct. This limits or clamps the output voltage to  $E_1$ :

$$v_o = E_1 \quad \text{for } v_s < E_1$$
 (4A.19)

If the output voltage is more than  $E_2$  then diode  $D_2$  cannot be reversed bias, and it turns on, limiting the output voltage to  $E_2$ :

$$v_o = E_2 \quad \text{for } v_s > E_2 \tag{4A.20}$$

A graph of the output is shown below:



Figure 4A.10

Limiting can also be achieved by exploiting the breakdown voltage of a Zener diode.

#### **Graphical Analysis of Clipping Circuit**

Consider the following circuit which clips at one level:



Figure 4A.11

Analysis is performed using a diode model We would like to consider the effect of a real diode and examine the output waveform for any particular input waveform. To do this we will use a piecewise linear model for the diode and draw the graph of the circuit's transfer function (i.e. a graph of output voltage versus input voltage).

First, we replace the diode with its model for the two cases of forward and reverse biased:



Figure 4A.12

Show that the diode conducts when:

$$v_s \ge E_1 + e_{fd} \tag{4A.21}$$

When the diode conducts, show that analysis of the forward biased equivalent circuit in Figure 4A.12 gives:

$$v_o = \frac{r_{fd}}{r_{fd} + R_s} v_s + \frac{R_s}{r_{fd} + R_s} \left( e_{fd} + E_1 \right)$$
(4A.22)

*Hint: use superposition (since there are two independent sources) and the voltage divider rule.* 

Show that for the reverse biased case:

$$v_o \approx v_s$$
 (4A.23)

*Hint: the resistance*  $r_{rd}$  *can be assumed to be much larger than*  $R_s$ *.* 

These two equations, corresponding to the two different states of the diode, give the relationship between the output voltage and source voltage. They are The transfer valid only in the region for which the diode model is valid, as determined by analysis of any input Eq. (4A.21). Graphing these two equations, in their appropriate regions, gives the transfer characteristic for the circuit:

characteristic allows waveform



Figure 4A.13

The effect this circuit has on a sine wave is shown.

#### **Summary**

- A peak detector charges a capacitor to the peak value of the input voltage. In normal operation, a load resistor normally exists on the output of the peak detector. In this case, the capacitor voltage decays exponentially until the input charges the capacitor again. This causes *ripple* in the output voltage.
- A clamp circuit maintains the integrity (shape) of the input waveform, but the DC level is shifted up or down, depending on the diode direction.
- Clipping or limiting circuits are used to endure that a voltage output is maintained within certain limits.

#### References

Sedra, A. and Smith, K.: *Microelectronic Circuits*, Saunders College Publishing, New York, 1991.

### **Problems**

#### 1.

Consider the clipping circuit shown opposite. Draw equivalent circuits for both forward and reverse biasing of the diode.



$$\hat{v}_i = 2(E - e_{fd}), \quad r_{fd} = \frac{R}{5}, \quad r_{rd} >> R,$$

 $v_i$ 

 $\wedge \quad \nabla^{v_o}$ 

 $D \sum_{E - \overline{}}$ 

and that E = 5 V and  $e_{fd} = 0.7$  V, use a graphical method to obtain  $v_o$ .

2.

Obtain expressions for Obtain expressions for<br/>the output voltage  $v_o$ , if: $K_s$ <br/> $v_1 \odot$  $v_o$ <br/> $v_2 \odot$ (i)  $v_1 = v_2 = V$  (DC) $R_s$ the output voltage  $v_o$ , if:

(ii) 
$$v_1 = V, v_2 = 0$$

Assume a constant voltage drop model, with  $e_{fd} = 0.7 \text{ V}$ .

3.



Sketch  $v_o$ . Indicate peak values.

4.

Determine V and I in the following circuits, when:

- a) The diodes are assumed to be ideal.
- b) The diodes are modelled with a constant voltage drop model with  $e_{fd} = 0.7 \text{ V}$ .

(i)



(ii)

