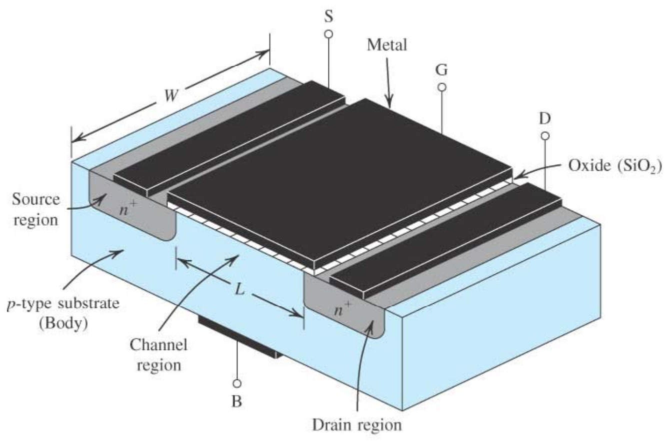
48521 FUNDAMENTALS of ELECTRICAL ENGINEERING

LECTURE 9A

The MOSFET

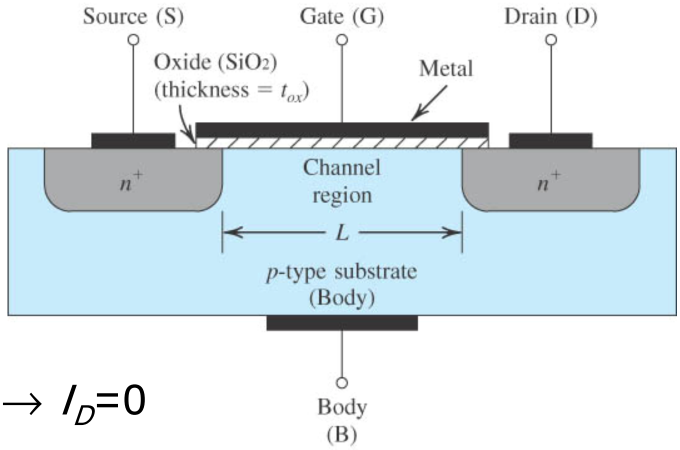
(Metal-Oxide-Semiconductor Field-Effect Transistor)

MOSFET: physical structure



(a)

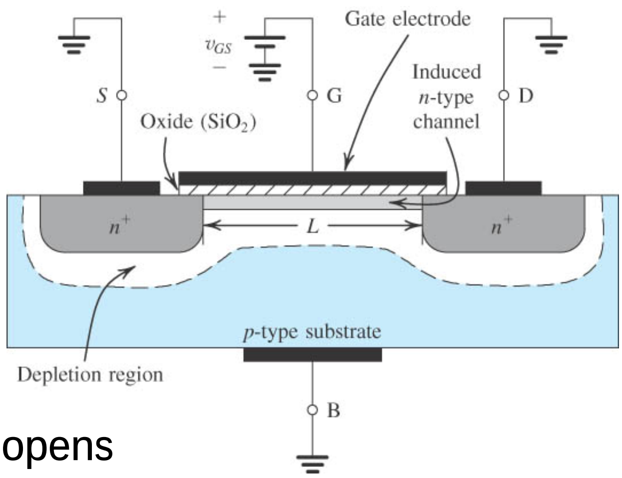
MOSFET (n-channel): operation



- $V_{GS} \le V_T \rightarrow I_D = 0$

MOSFET (n-channel): operation

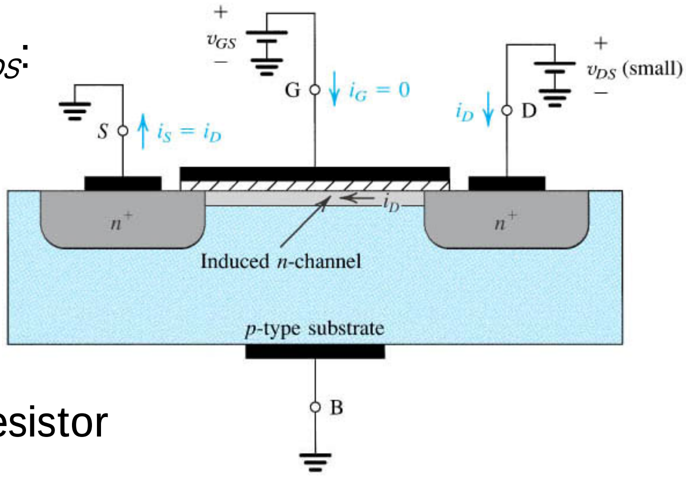
- $V_{GS} > V_T$



- A channel opens

MOSFET (n-channel): operation

- Small V_{DS}:



- Linear resistor

MOSFET (n-channel): operation

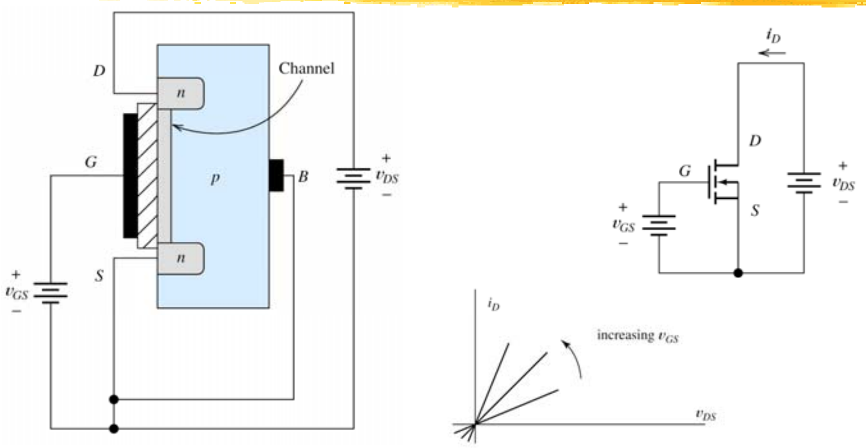
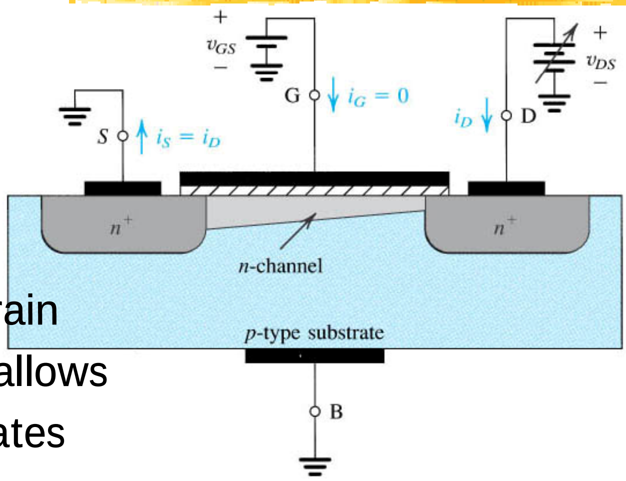


Figure 12.4 For $v_{GS} > V_{to}$, a channel of n-type material is induced in the region under the gate. As v_{GS} increases, the channel becomes thicker. For small values of v_{DS}, i_D is proportional to v_{DS}. The device behaves as a resistance whose value depends on v_{GS}.

MOSFET (n-channel): operation

- Larger V_{DS}:
- Near the drain channel shallows
- $\rightarrow$ I_D saturates



MOSFET: output characteristics

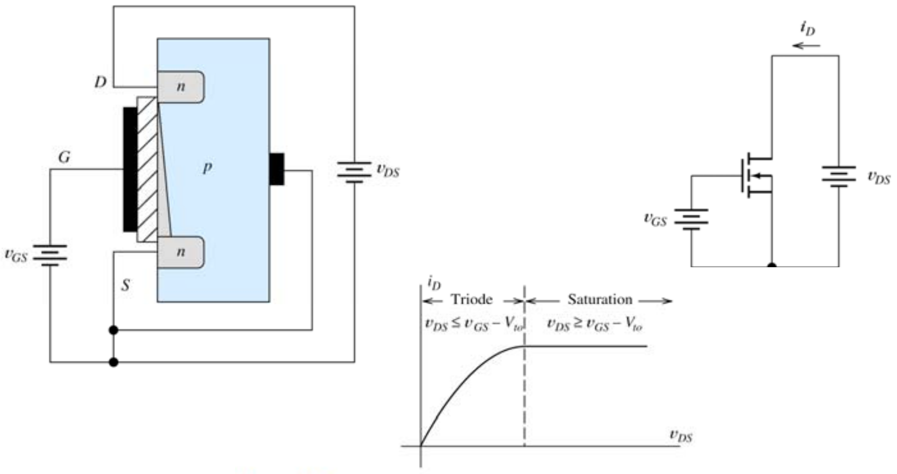


Figure 12.5 As v_{DS} increases, the channel pinches down at the drain end and i_D increases more slowly. Finally, for $v_{DS} > v_{GS} - V_{to}$, i_D becomes constant.

MOSFET: output characteristics

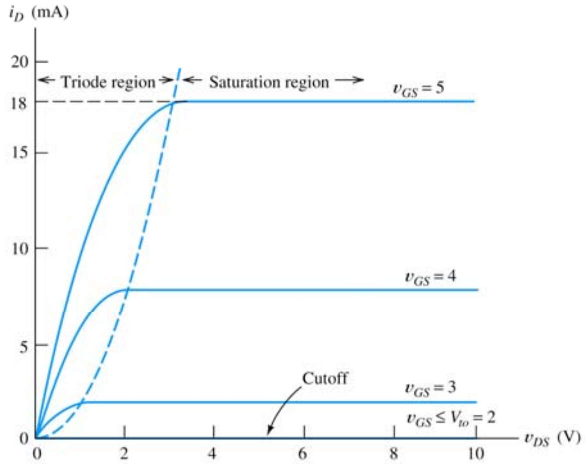
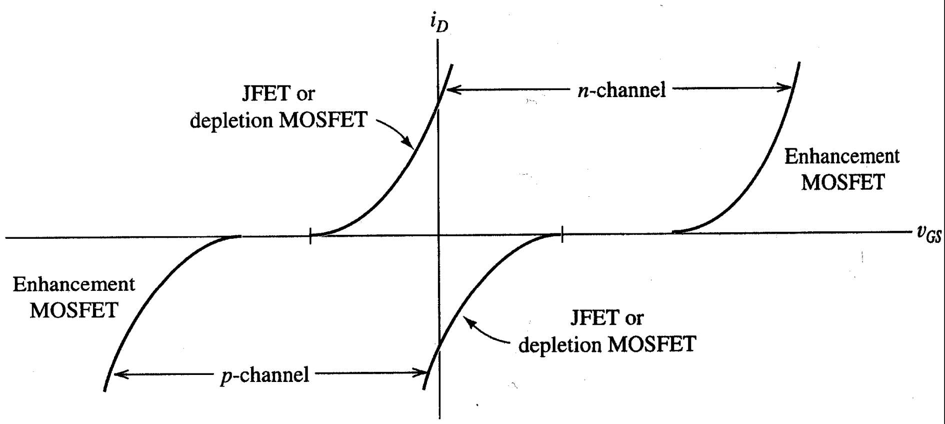


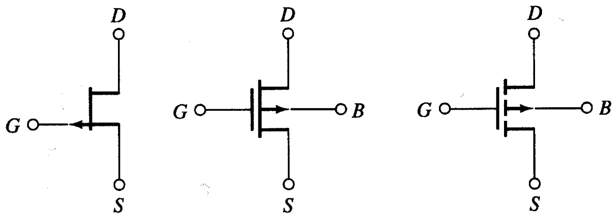
Figure 12.6 Characteristic curves for an NMOS transistor.

FET: transfer characteristics



FET: circuit symbols

- *p*-channel devices:



(a) JFET (b) Depletion MOSFET (c) Enhancement MOSFET

- For *n*-channel devices, reverse the arrows

FET Model (Large-Signal)

- Both FETs (JFET and MOSFET) can be described by mathematically identical equations:

$$i_D = \begin{cases} K\left[2\left(v_{GS} - V_t\right) - v_{DS}\right]v_{DS} \text{ ; } v_{DS} \le v_{GS} \text{ - } V_t \\ K\left(v_{GS} - V_t\right)^2 \text{ ; } v_{DS} > v_{GS} \text{ - } V_t \end{cases}$$

FET Model (Large-Signal)

- For JFETs: $K \leftarrow \frac{I_{DSS}}{V_p^2}$; $V_t \leftarrow V_p$ (pinch – off voltage)
- For MOSFETs: $K \leftarrow \frac{\mu C_{ox}}{2}\frac{W}{L}$

μ – carrier mobility

C_{ox} – oxide capacitance [F/m^2]

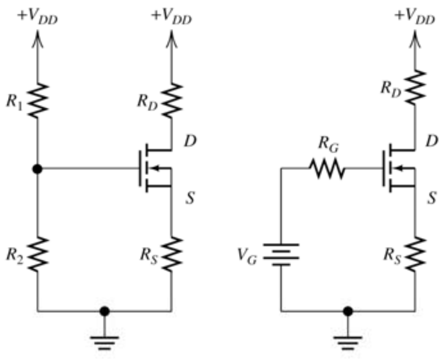
W, L - channel width and length

MOSFET: biasing

- Voltage divider
- Drain-Gate feedback
- Current source
- Self-bias
- Zero-bias (depletion type only)

MOSFET biasing: voltage divider

- $R_G = R_1R_2/(R_1+R_2)$
- R_G very large (~ MΩ)
- $i_G = 0 \rightarrow$
- $\rightarrow V_G = V_{DD}R_2/(R_1+R_2)$
- $i_G = 0 \rightarrow i_D = i_S$
- $v_{GS} = V_G - i_D{*}R_S$
- $v_{DS} = V_{DD} - i_D{*}(R_D+R_S)$



(a) Original circuit (b) Gate bias circuit replaced by its Thévenin equivalent

Figure 12.13 Fixed- plus self-bias circuit.

MOSFET biasing: voltage divider

- To find the operating point we usually assume that the device operates in the saturation region, i.e.:

$$i_D = K(v_{GS} - V_t)^2$$

- But we also have:

$$v_{GS} = V_G - i_D R_S \; ; \quad v_{GS} > V_t$$

MOSFET biasing: voltage divider

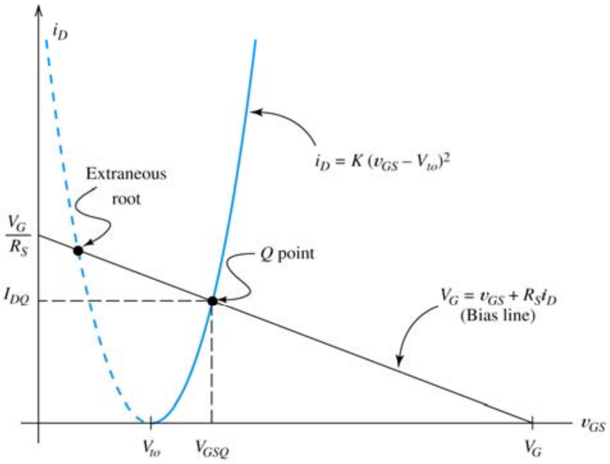


Figure 12.14 Graphcial solution of Equations 12.12 and 12.13.

MOSFET biasing: voltage divider

- Now, we have to solve for v_{GS}:

$$V_G = v_{GS} + R_S K (v_{GS} - V_t)^2$$

- or

$$R_S K v_{GS}^2 + (1 - 2V_t R_S K) v_{GS} + R_S K V_t^2 - V_G = 0$$

- This quadratic equation has two solutions; we must accept only $v_{GS} > V_t$

MOSFET biasing: voltage divider

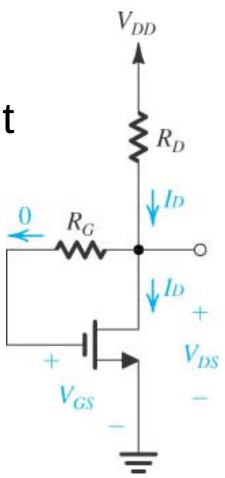
- Once v_{GS} is known, we calculate i_D:

$$i_D = K(v_{GS} - V_t)^2$$

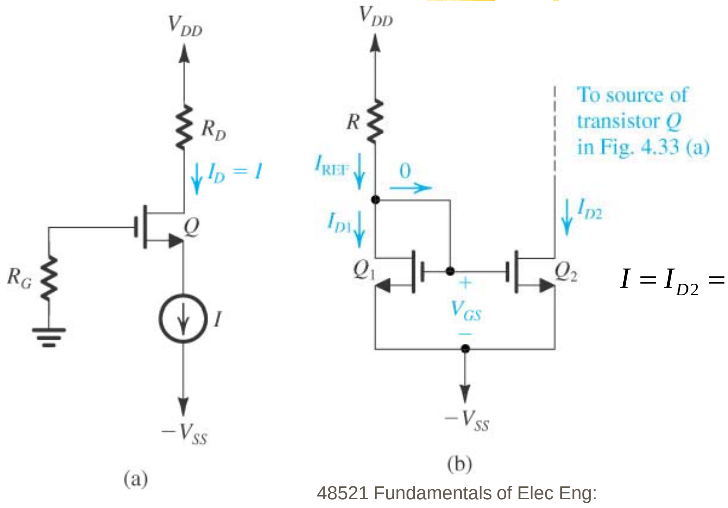
- and $v_{DS} = V_{DD} - i_D*(R_D+R_S)$
- Finally, we must check if $v_{DS} > v_{GS} - V_t$
- If not, the MOSFET is NOT in saturation !
- Repeat, assuming triode (linear) region.

MOSFET biasing: drain-gate feedback

- Here $v_{GS} = v_{DS}$
- In an *n*-channel enhancement MOSFET V_t>0
- So, the saturation condition $v_{DS} > v_{GS} - V_t$ is **always** satisfied
- $v_{DS} = V_{DD} - R_D K(v_{DS} - V_t)^2$



MOSFET biasing: current source (mirror)



$$I = I_{D2} = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$