

## Lecture 9A – The Bipolar Junction Transistor

*Principle of the Bipolar Junction Transistor (BJT). Biasing circuit. Small signal equivalent circuit. Common emitter voltage amplifier. The emitter follower.*

### Principle of the Bipolar Junction Transistor (BJT)

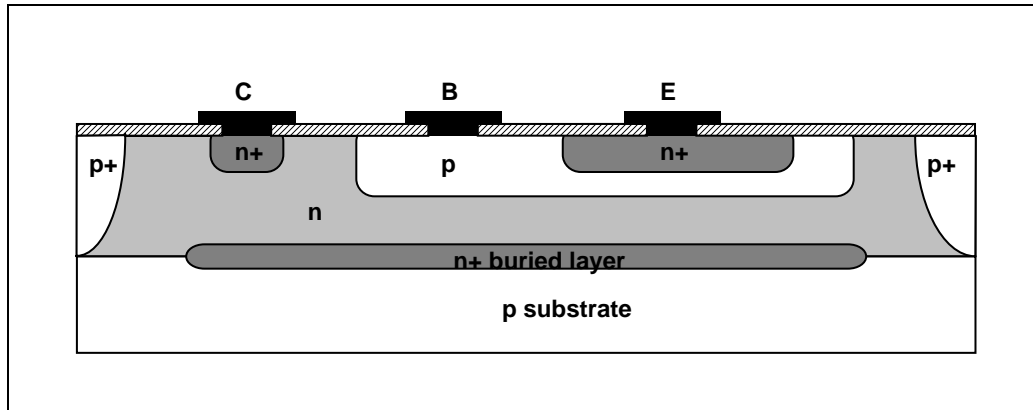
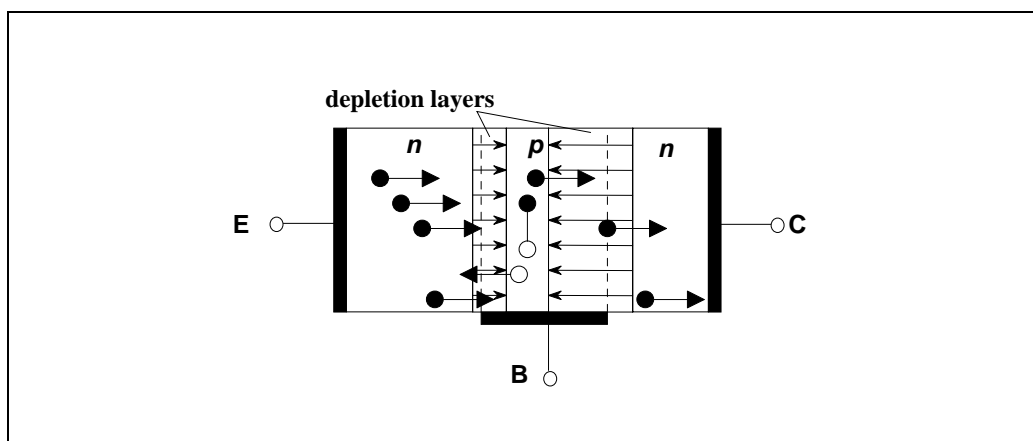


Figure 9A.1

A bipolar junction transistor is formed by the following process. Starting with a p-type substrate, a layer of heavily doped n-type material is deposited. This is the buried layer, and forms a low resistance path for what we will eventually call the collector current. An epitaxial layer of n-type semiconductor is deposited on top.

Isolation diffusion is then used to isolate the transistor. A base region is formed by very lightly diffusing p-type silicon into the structure. The emitter is formed by heavy n-type diffusion into the base. The result is an *npn* transistor.

We can simplify the above geometry to the following:



## 9A.2

**Figure 9A.2**

The base-emitter junction (EBJ) is forward biased and the base-collector junction is reverse biased for "active mode" operation.

The forward bias on the EBJ causes a current across the junction. Electrons, which are the majority carriers in the emitter, are "injected" into the base. The base is lightly doped, so only some of the electrons will recombine with holes (the majority carriers in the base). The electrons in the base will be like gas molecules - they will diffuse in the direction of the concentration gradient - away from the EBJ. When they reach the collector-base depletion region, they are swept across by the field existing there (hence the electrons are collected).

The collector current is therefore seen to be independent of the CBJ reverse bias voltage. All that is necessary is a field of some magnitude between the collector and base.

There are two components to the base current. One is the holes injected from the base into the emitter. The other represents the holes that enter the base and recombine with electrons.

The charge carriers in the BJT are electrons and holes, hence the name bipolar junction transistor.

The collector current is almost equal to the current due to the forward biased EBJ, so it has an exponential relationship with  $v_{BE}$ . The base current, consisting almost entirely of injected holes, is much smaller, but still has an exponential relationship with  $v_{BE}$ . The collector current and base current are therefore proportional:

$$i_c = \beta i_b$$

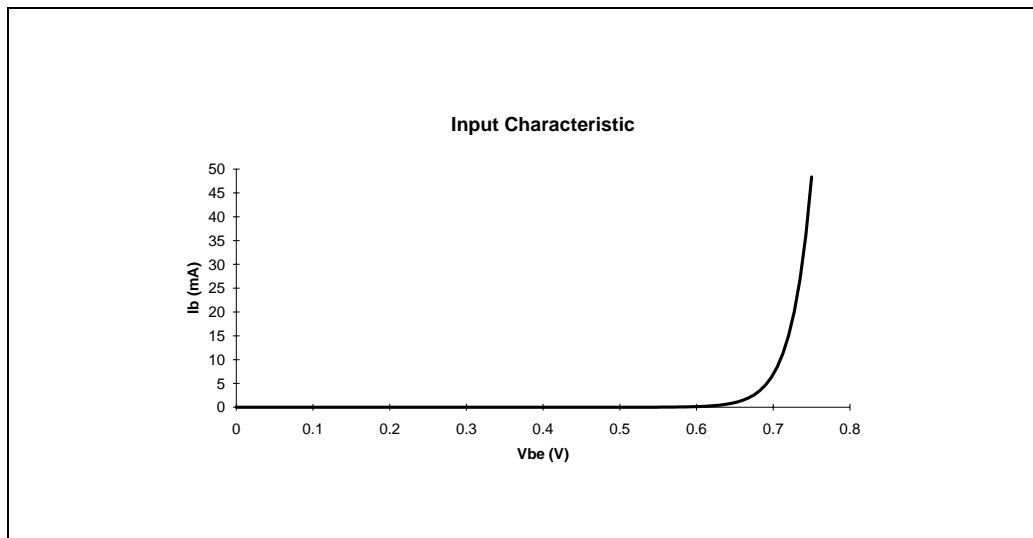
$\beta$  = common - emitter current gain (9A.1)

We can now look at the characteristics and explain their shape.

## Input and Output Characteristics

The input characteristic is a graph of input current vs voltage, i.e.  $I_B$  vs  $V_{BE}$ .

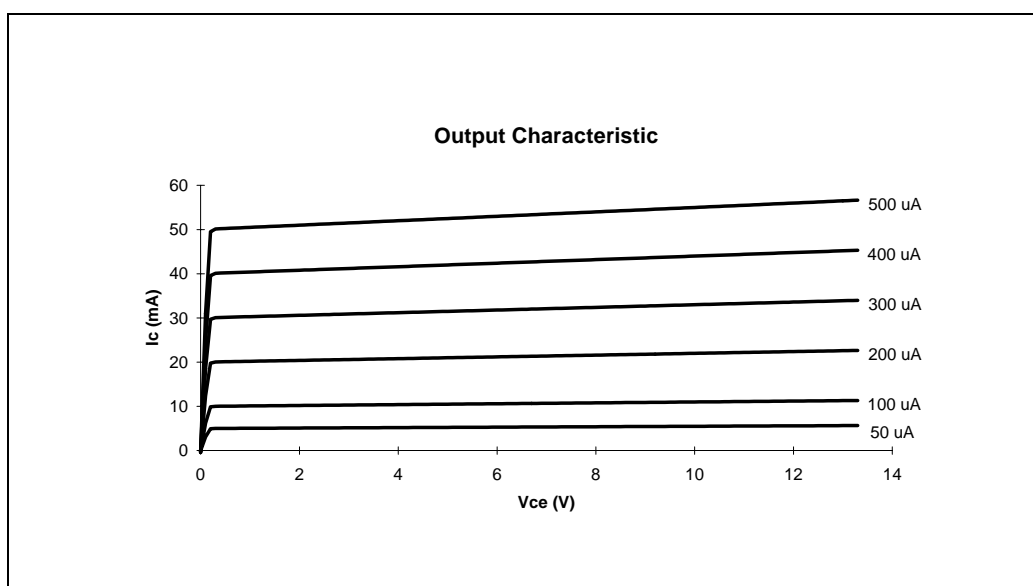
It is equivalent to a forward biased  $p$ - $n$  junction:



**Figure 9A.3**

The slope at a point on the characteristic is the inverse of the small signal input resistance of the device.

The output characteristic is a graph of  $I_C$  vs  $V_{CE}$  for particular values of  $I_B$ . It is similar to the MOSFET output characteristic, except now the output current is controlled by a current (instead of a voltage). By varying  $I_B$  we obtain a family of characteristics:



**Figure 9A.4**

## 9A.4

In the active region, the collector current is nearly independent of the collector-emitter voltage. It is therefore like a current source. The collector current is set by the base current.

The slope of the curve in the active region is the inverse of the small signal output resistance of the device.

### Biasing Circuit

To use the BJT as an amplifier, we must ensure that it is in the active mode. The EBJ must be forward biased and the CBJ must be reverse biased. The biasing circuit should minimize the effect of transistor parameter variations. These may be caused by varying devices or changes in temperature.

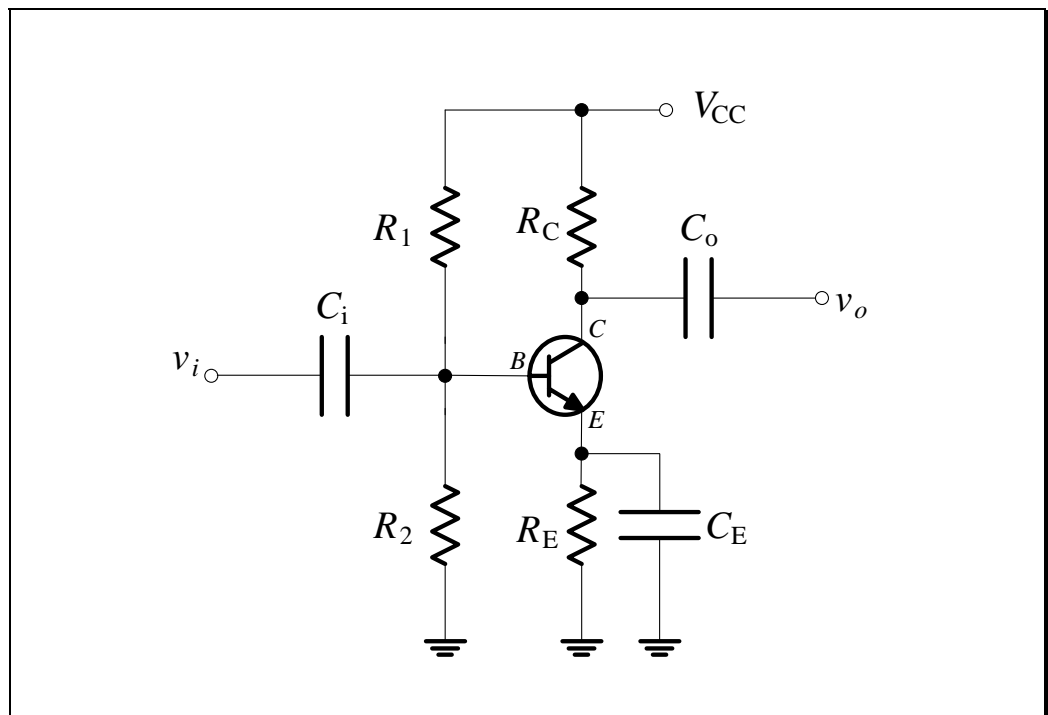


Figure 9A.5

Suppose we have chosen the  $Q$  point ( $I_{CQ}$  and  $V_{CEQ}$ ). We now wish to design the bias circuit. The capacitors block all DC components of current and are equivalent to short circuits for AC. They are not considered in the DC analysis of the bias circuit.

The purpose of  $R_E$  is to make the bias voltage  $V_B = V_{BE} + V_E$  just large enough to be not affected by variations in  $V_{BE}$  (due to temperature) and  $r_{be}$  (due to device variations).

As  $V_{BE} \approx 0.7$  V for silicon, we choose  $V_E = 1$  V (no larger than 2 V). Therefore:

$$I_E = I_C + I_B \quad (9A.2a)$$

$$\approx I_{CQ} \quad (9A.2b)$$

$$R_E = \frac{V_E}{I_{CQ}} = \frac{1}{5} = 200 \, \Omega \quad (9A.2c)$$

KVL from ground, through the BJT, to the DC supply gives:

$$V_E + V_{CEQ} + R_C I_C = V_{CC} \quad (9A.3)$$

We choose  $I_C$  so that there can be equal positive and negative voltage excursions at the collector:

$$R_C I_C = V_{CEQ} \quad (9A.4)$$

$$R_C = \frac{V_{CEQ}}{I_{CQ}} = \frac{10}{5} = 2 \, \text{k}\Omega$$

Therefore, the supply voltage will have to be  $V_{CC} = 10 + 10 + 1 = 21$  V.

We would like to keep the input resistance to the amplifier large, so we want to choose the resistors  $R_1$  and  $R_2$  as large as possible. However, to keep the voltage at the base independent of the transistor parameters (the base current  $I_B$  will vary between devices for a given  $I_C$ ), we want the current in the potential divider to be larger than the base current.

## 9A.6

A trade off is necessary, so we choose the current through  $R_1$  and  $R_2$  to be  $0.1I_{CQ}$ :

$$R_1 + R_2 = \frac{V_{CC}}{0.1I_{CQ}} = \frac{21}{0.5} = 42 \text{ k}\Omega \quad (9A.5)$$

To obtain the individual values, we apply KVL around the base-emitter loop:

$$R_2 0.1I_{CQ} - V_{BE} - V_E = 0$$

$$R_2 = \frac{V_{BE} + V_E}{0.1I_{CQ}} = \frac{1.7}{0.5} = 3.4 \text{ k}\Omega \quad (9A.6a)$$

$$R_1 = 42 - 3.4 = 38.6 \text{ k}\Omega \quad (9A.6b)$$

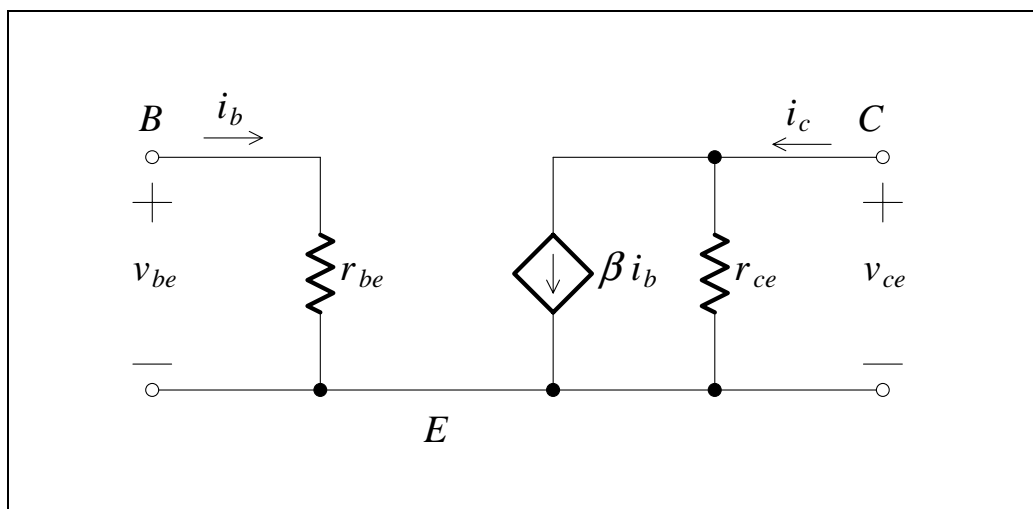
## Small Signal Equivalent Circuit

From the output characteristic, we can see that the output current is controlled by  $i_b$  and  $v_{ce}$ :

$$i_c = \beta i_b + y_{ce} v_{ce} \quad (9A.7)$$

This is valid for mid frequencies, where we can ignore the  $p$ - $n$  junction capacitances.

The small signal equivalent circuit is therefore:



**Figure 9A.6**

Notice how the dependent source in this model is current controlled. We can make it voltage controlled by saying:

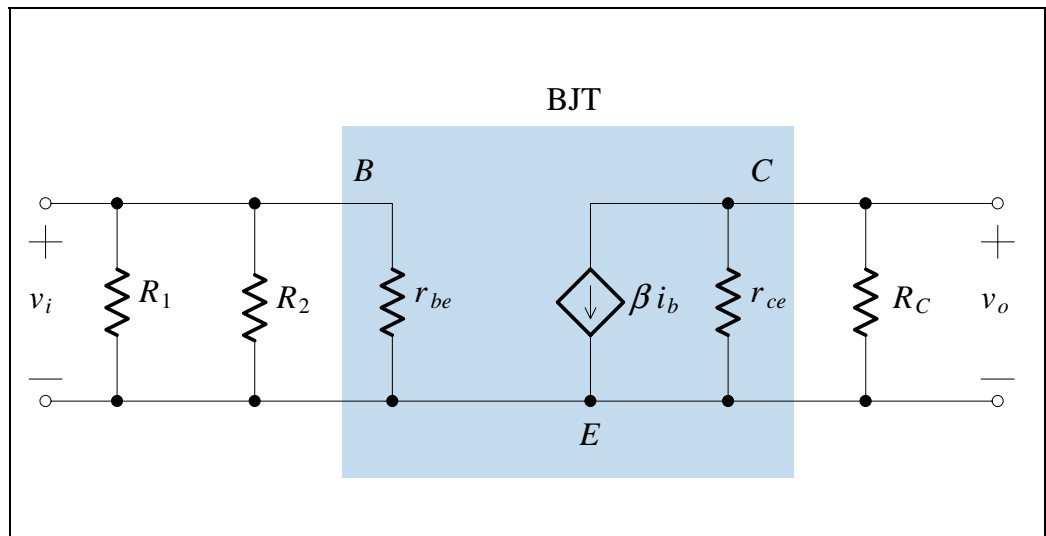
$$\begin{aligned} \beta i_b &= g_m v_{be} = g_m r_{be} i_b \\ \therefore g_m &= \frac{\beta}{r_{be}} \end{aligned} \quad (9A.8)$$

# 9A.8

## Common Emitter Voltage Amplifier

For small AC signals, the BJT small signal equivalent circuit can be used in the AC analysis. We note also that the capacitor  $C_E$  by-passes (effectively shorts) the resistor  $R_E$ . The DC supply is equivalent to a short circuit so that resistor  $R_C$  is connected to common. The input and output capacitors  $C_i$  and  $C_o$  are assumed to have zero reactance. It is very similar to the MOSFET common source voltage amplifier.

The small signal AC equivalent circuit becomes:



**Figure 9A.7**

The parameters of the voltage amplifier we need for our "amplifier block" representation are:

$$A_{vo} = \frac{v_o}{v_i} = -\frac{\beta i_b (r_{ce} \parallel R_C)}{i_b r_{be}}$$

$$\approx -\frac{\beta}{r_{be}} R_C = -g_m R_C \quad (9A.9a)$$

$$R_{in} = R_1 \parallel R_2 \parallel r_{be} \quad (9A.9b)$$

$$R_{out} = r_{ce} \parallel R_C \approx R_C \quad (9A.9c)$$



## The Emitter Follower

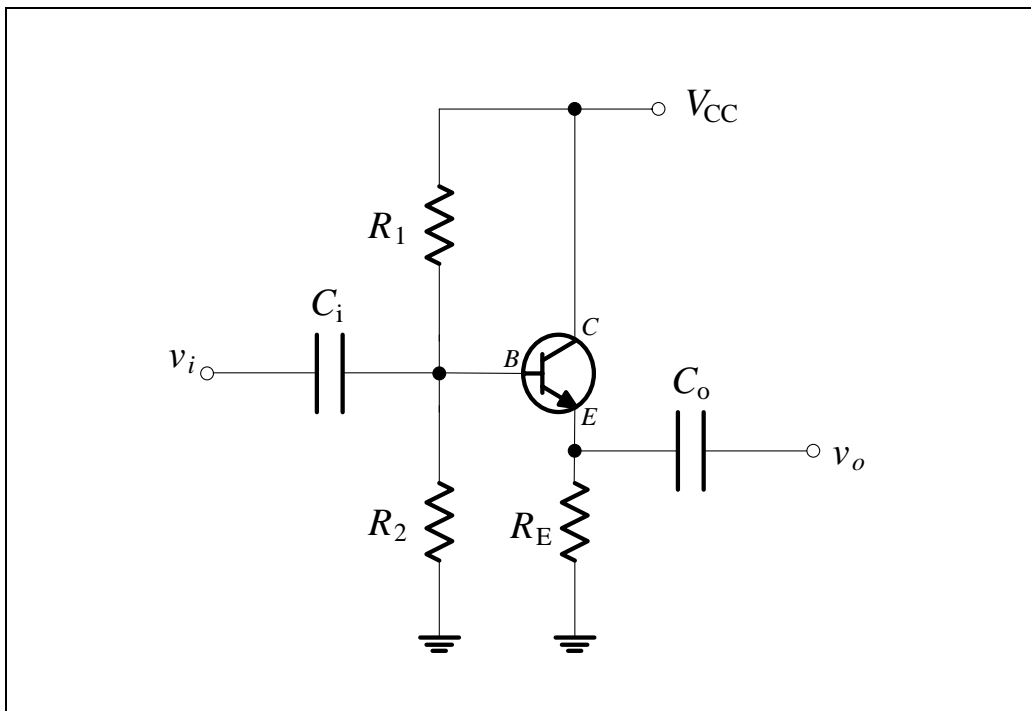


Figure 9A.8

Here, the output is taken from the emitter terminal, and the collector, for AC is connected to the common.

The small signal equivalent circuit for the above amplifier is:

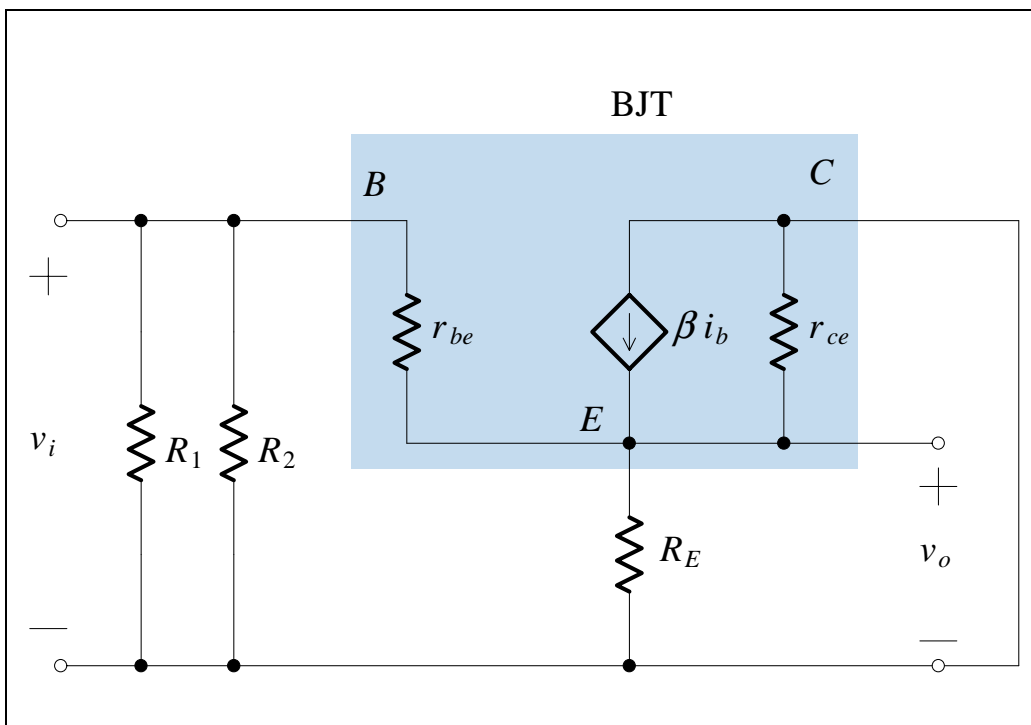


Figure 9A.9

## 9A.10

KCL at the emitter gives:

$$\begin{aligned}
 \beta i_b + i_b &= \frac{v_o}{r_{ce} \parallel R_E} \\
 (\beta + 1) \frac{v_i - v_o}{r_{be}} &= \frac{v_o}{r_{ce} \parallel R_E} \\
 \frac{v_i}{r_{be}/(\beta + 1)} &= \left( \frac{1}{r_{ce} \parallel R_E} + \frac{1}{r_{be}/(\beta + 1)} \right) v_o \\
 \frac{v_o}{v_i} &= \frac{1}{\frac{r_{be}/(\beta + 1)}{r_{ce} \parallel R_E} + 1} \\
 A_{vo} &= \frac{r_{ce} \parallel R_E}{r_{ce} \parallel R_E + r_{be}/(\beta + 1)} \approx 1
 \end{aligned} \tag{9A.10}$$

KVL at the base gives:

$$\begin{aligned}
 v_b &= r_{be} i_b + (r_{ce} \parallel R_E)(\beta + 1) i_b \\
 R_{in} = \frac{v_b}{i_b} &= r_{be} + (r_{ce} \parallel R_E)(\beta + 1) = \text{large}
 \end{aligned} \tag{9A.11}$$

We can first find the short circuit current, and using the open circuit voltage, find the output resistance:

$$\begin{aligned}
 i_{sc} &= (\beta + 1) i_b = (\beta + 1) \frac{v_i}{r_{be}} \\
 R_{out} = \frac{v_{oc}}{i_{sc}} &= \frac{r_{ce} \parallel R_E}{r_{ce} \parallel R_E + r_{be}/(\beta + 1)} \frac{r_{be}}{(\beta + 1)} \\
 &= r_{be}/(\beta + 1) \parallel r_{ce} \parallel R_E = \text{small}
 \end{aligned} \tag{9A.12}$$

## References

Sedra, A. and Smith, K.: *Microelectronic Circuits*, Saunders College Publishing, New York, 1991.