Lecture 11A – The Operational Amplifier

The MOS differential pair. Common mode rejection ratio (CMRR). The operational amplifier.

The MOS Differential Pair

The differential-pair is the most important amplifier configuration in analog integrated circuits. It has two inputs and two outputs. Its usefulness is derived from one basic property: it amplifies the difference in voltage that may exist between its two input terminals. This property will turn out to be extremely desirable when we look at the operational amplifier, and the use of "feedback".

Differential circuits are much less sensitive to noise and interference than single-ended circuits. Also, the differential configuration enables us to bias the amplifier and to cascade amplifier stages without the need for bypass and decoupling capacitors, thus allowing circuit miniaturisation onto an IC.

The MOS differential pair

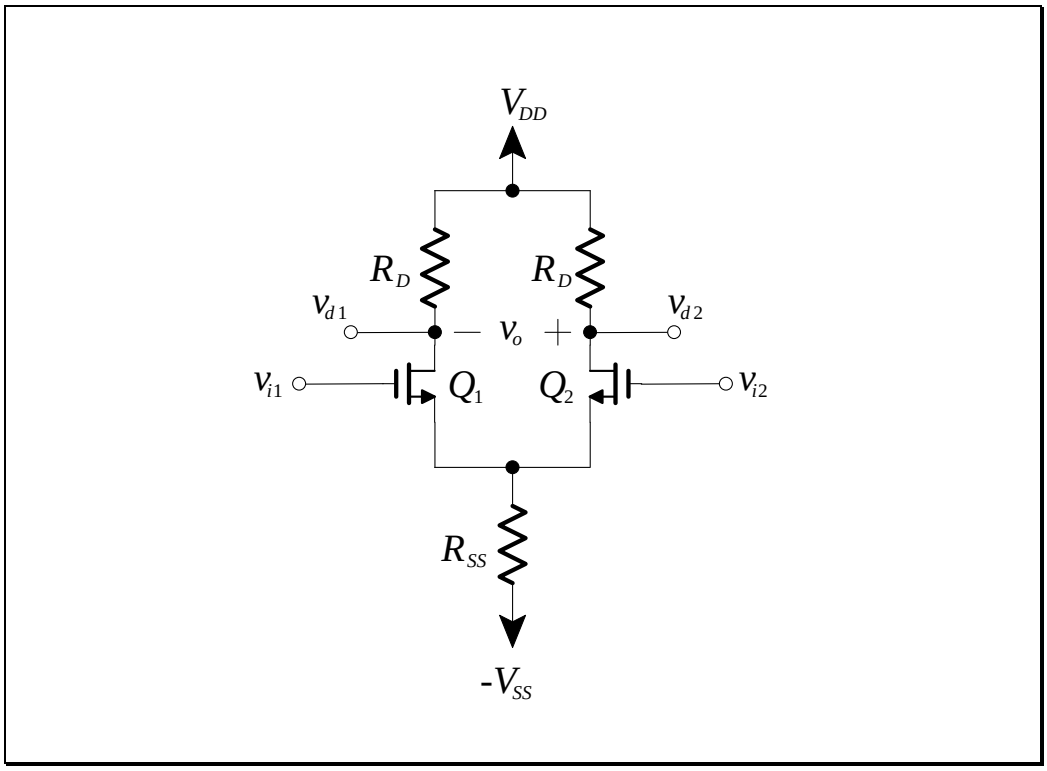


Figure 11A.1

For the circuit to work, it is critical that the two sides of the amplifier behave in exactly the same way. This means the transistors and resistors must be "matched" so that the circuit is perfectly symmetric.

11A.2

DC Conditions

For DC conditions, the signals at the gates are set (using superposition) to zero – the gate of each transistor is "tied to the common".

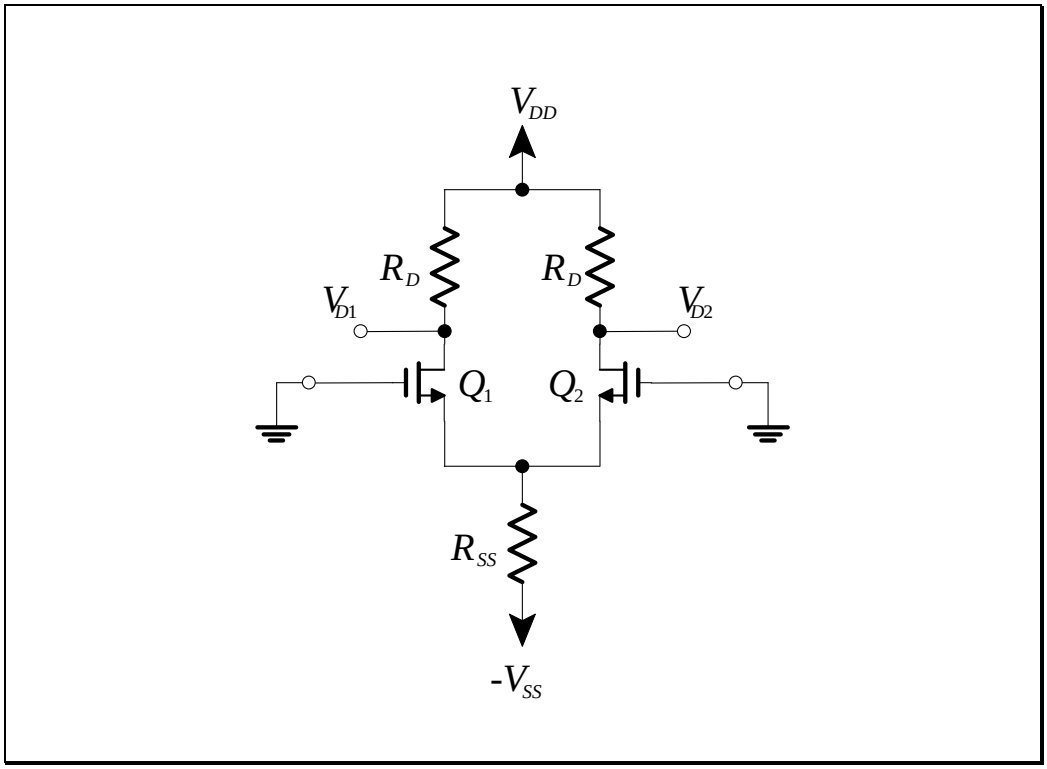


Figure 11A.2

Now assume that the transistors are conducting and are in the saturation region of operation. Then since the two transistors are matched, and since they have the same gate-source voltage, the drain currents will be the same. Hence the voltage at the drains will be the same.

$$V_{D1} = V_{D2} = V_{DD} - R_D I_D \tag{11A.1}$$

The output is taken differentially between the two collectors, so there will be no DC output voltage (0 V).

AC Conditions

Any two inputs we apply at the gates can be thought of as the superposition of two types of voltage: an average and a difference.

We call the average value of the two signals the common-mode voltage, and the difference between the two signals the differential voltage:

$$\text{common mode voltage} \quad v_{icm} = \frac{v_{i1} + v_{i2}}{2} \tag{11A.2a}$$

$$\text{differential voltage} \quad v_{id} = v_{i1} - v_{i2} \tag{11A.3b}$$

The individual applied signals can be expressed as functions of the common mode voltage and differential mode voltage:

$$v_{i1} = v_{icm} + \frac{v_{id}}{2} \tag{11A.3a}$$

$$v_{i2} = v_{icm} - \frac{v_{id}}{2} \tag{11A.3b}$$

Any input signal we consider will be decomposed into these two types of signal, to simplify analysis of the circuit. We can find the gain of the amplifier for each type of signal, and use superposition to obtain the overall output voltage:

$$A_d = \text{differential OC voltage gain} \tag{11A.4a}$$

$$A_{cm} = \text{common - mode OC voltage gain} \tag{11A.4b}$$

$$v_o = A_d v_{id} + A_{cm} v_{icm} \tag{11A.4c}$$

11A.4

Common-Mode

For small signals, we carry out ordinary circuit analysis using the small signal equivalent circuit for each MOSFET:

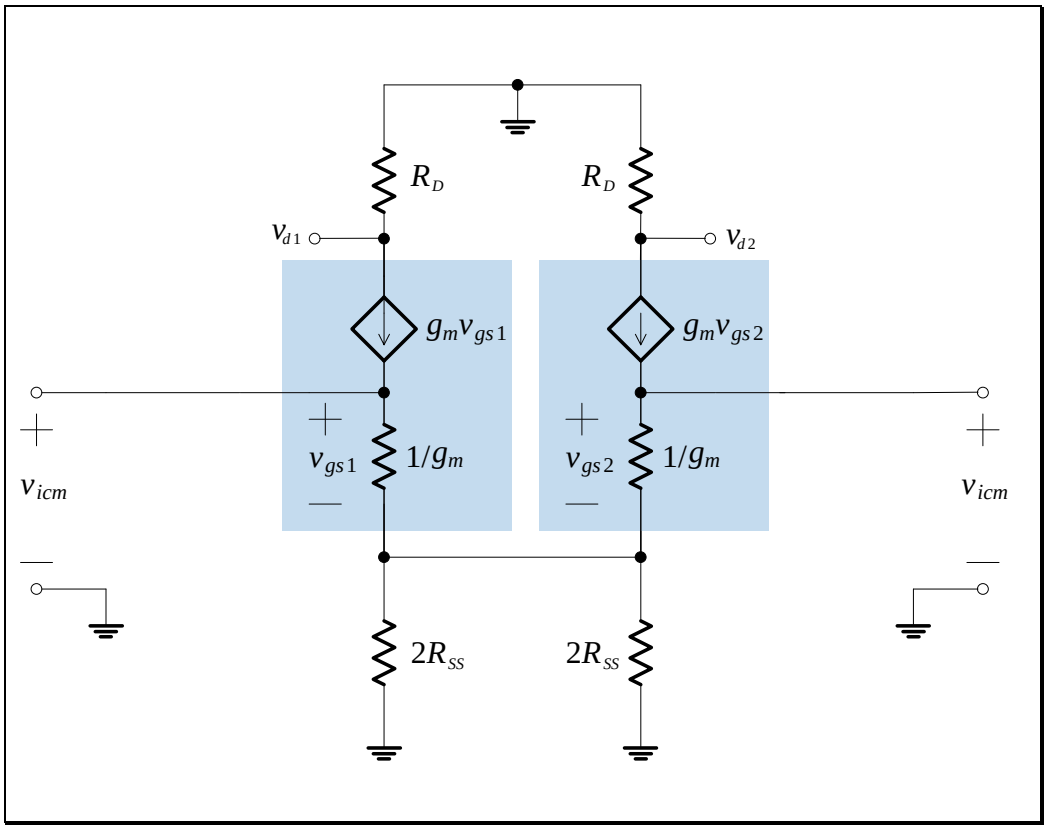


Figure 11A.3

Note that the resistor R_{SS} has been split into two parallel resistors of value $2R_{SS}$. The transistors have exactly the same voltage between gate and source, which implies that the drain currents must be identical. Because of the symmetry of the circuit, there is no current in the lead connecting the two sources. The circuit behaviour is unchanged if this lead is removed. When this is done, the circuit reduces to two "half-circuits" that are completely independent.

Only one of the half circuits needs to be analyzed to predict circuit behaviour:

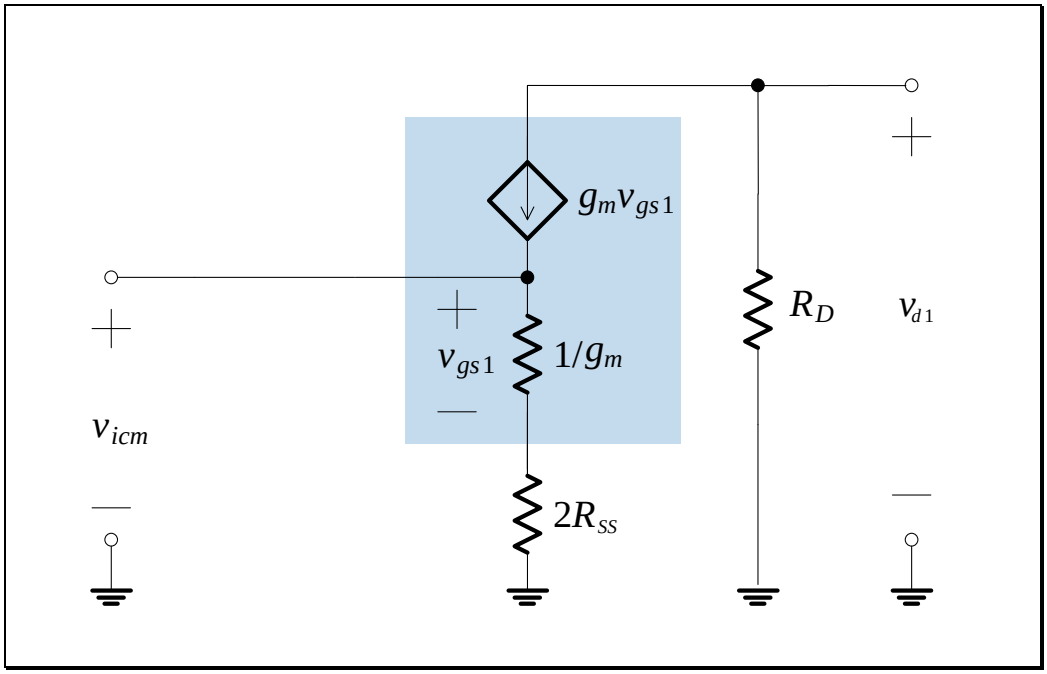


Figure 11A.4

The voltage divider rule at the input gives:

$$v_{gs1} = \frac{1/g_m}{1/g_m + 2R_{SS}} v_{icm} \qquad (11A.5)$$

The common-mode output voltage is given by Ohm's law:

$$\begin{aligned} v_{d1} &= -R_D g_m v_{gs1} \\ &= \left[\frac{-R_D}{1/g_m + 2R_{SS}} \right] v_{icm} \end{aligned} \qquad (11A.6)$$

If the output is taken differentially, then the output common-mode voltage $v_o \equiv v_{d2} - v_{d1}$ will be zero. On the other hand, if the output is taken single-endedly (say, between the drain of Q_1 and common), then the common-mode gain A_{cm} will be finite and given by:

$$A_{cm} = \frac{v_{d2}}{v_{icm}} = \frac{-R_D}{1/g_m + 2R_{SS}} \approx \frac{-R_D}{2R_{SS}} \qquad (11A.6)$$

To make the common-mode voltage gain small, we choose the resistor R_{SS} to be very large. Ideally, it would be infinite, and the transistors would be biased using a current source.

This common-mode output voltage only appears when we take the output from a single drain to common (we eventually want our output signal referenced to common). If we take the output differentially, then the common-mode voltage gain will be zero. Integrated circuits utilizing several differential pairs have the output of the first differential pair connected to the input of a second differential pair to increase rejection of common-mode signals.

In real integrated circuits it is impossible to exactly match the components on both sides of the differential pair, so there will always be some finite (but small) common-mode gain, even if the output is taken differentially.

Differential Mode

We again carry out the usual circuit analysis using the small signal equivalent circuit model for the MOSFET:

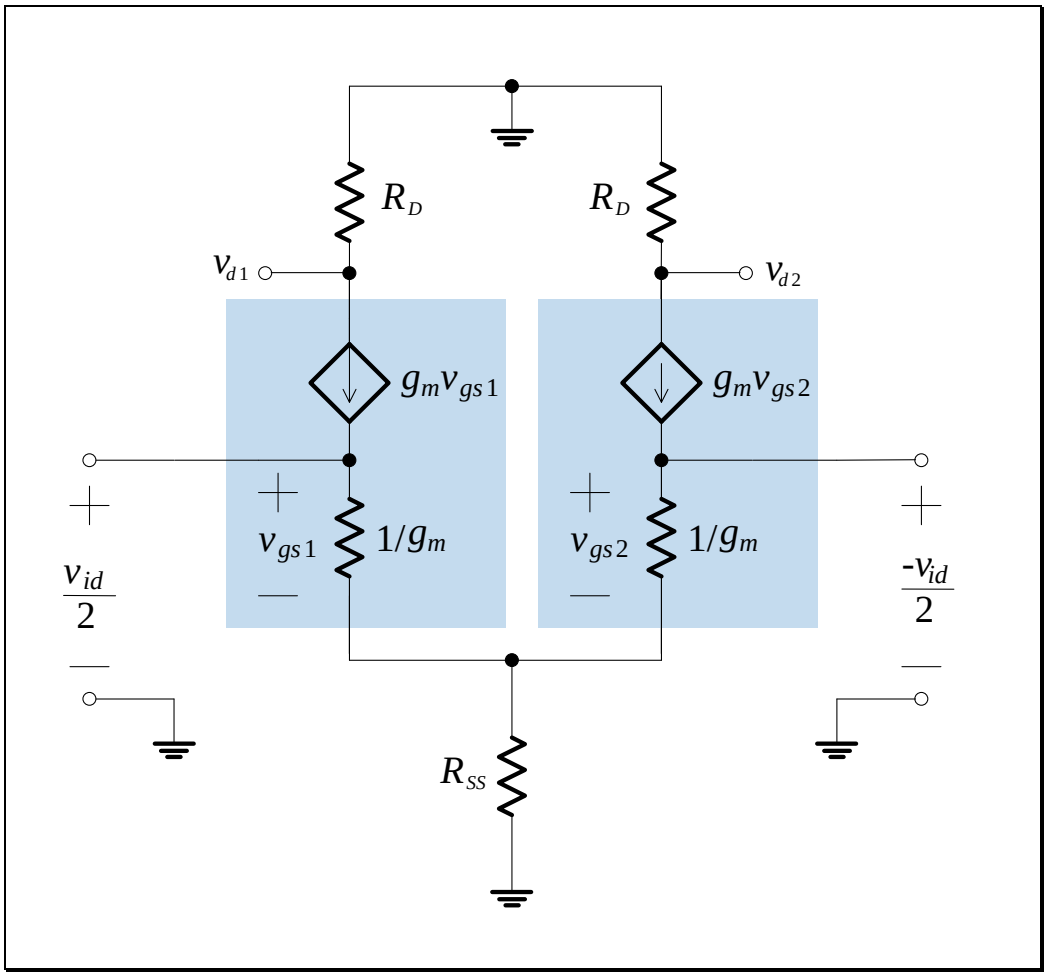


Figure 11A.5

By symmetry arguments the voltage at the sources must be zero. To see this, use superposition. Let the voltage at the source be v_{s1} due to the input $v_{id}/2$, with the other source set to zero. Then the voltage at the source due to the input $-v_{id}/2$ must be $-v_{s1}$ (the circuit is linear). The superposition of the two voltages leads to 0 V. Therefore, the resistor R_{SS} may be shorted without affecting circuit behaviour.

The equivalent circuit then becomes:

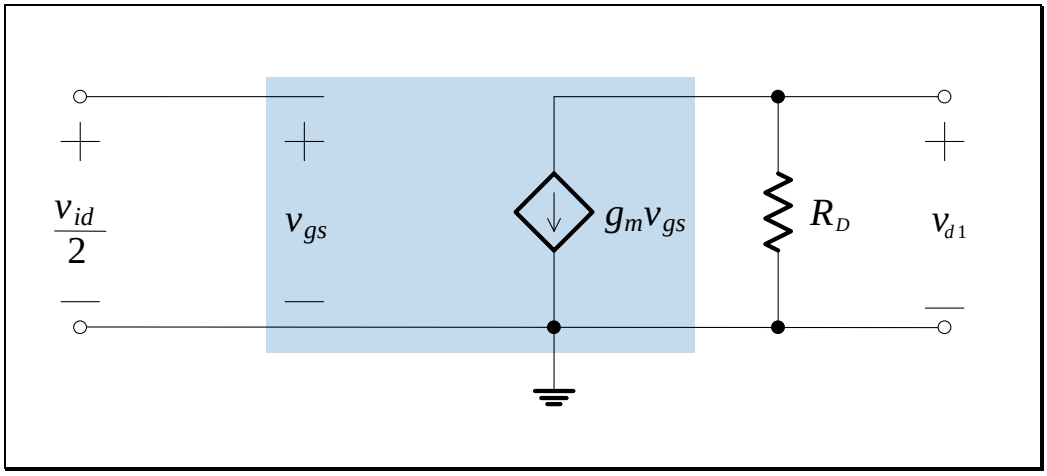


Figure 11A.6

The output voltage is given by Ohm's law:

$$v_{d1} = -\frac{1}{2} g_m R_D v_{id} \tag{11A.7}$$

If the output is taken differentially, then the differential gain will be:

$$A_d = \frac{v_{d2} - v_{d1}}{v_{id}} = g_m R_D \tag{11A.8}$$

On the other hand, if we take the output single-endedly, then the differential gain will be given by:

$$A_d = \frac{v_{d2}}{v_{id}} = \frac{1}{2} g_m R_D \tag{11A.9}$$

Common-Mode Rejection Ratio

A measure of the differential pair's circuit quality is the common-mode rejection ratio. It is defined as:

$$CMRR = \frac{|A_d|}{|A_{cm}|} \qquad \text{(11A.10a)}$$

$$CMRR\,(\text{dB}) = 20\log\frac{|A_d|}{|A_{cm}|} \qquad \text{(11A.12b)}$$

Ideally, we would like A_{cm} to be zero so that we have infinite common-mode rejection.

For a perfectly matched differential pair, the common-mode rejection ratio for the output taken single-endedly is:

$$CMRR = \frac{|A_d|}{|A_{cm}|} \approx \frac{\frac{1}{2} g_m R_D}{R_D / 2R_{SS}} = g_m R_{SS} \qquad \text{(11A.11)}$$

The Operational Amplifier

Operational amplifiers (op-amps) are integrated circuit amplifiers consisting of several stages, fabricated within the top 10 μm of a 250 μm *Si* chip. Op-amps amplify the voltage difference between the two inputs. External components are connected by conductive paths in the silicon. Internally DC coupling is used and bulky passive elements (capacitors) are avoided. The complete device is small, cheap, has very high gain, wide bandwidth and a large operating temperature range ($A \approx 2 \times 10^5$, $R_i \approx 2$ MΩ, $R_o \approx 75$ Ω).

For *general-purpose* ope-amps, BJT differential pairs are mostly used at the input because they are easy to match, have a good CMRR and are capable of carrying larger currents than FETs. However, some operational amplifiers have a FET input, with the rest of the circuit being made from BJTs.

CMOS op-amps find application in the design of analog and mixed-signal very large scale integrated (VLSI) circuits.

The symbol of the operational amplifier is:

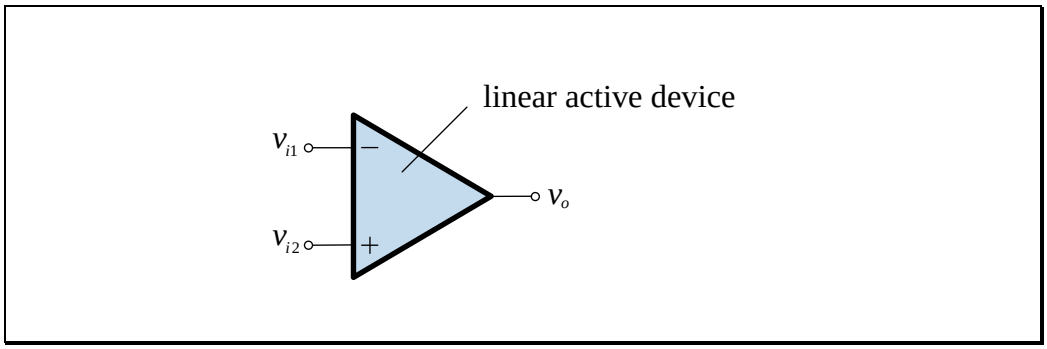


Figure 11A.7

The operational amplifier also has a common-mode gain and a differential gain. We can use superposition to find the output for any given input:

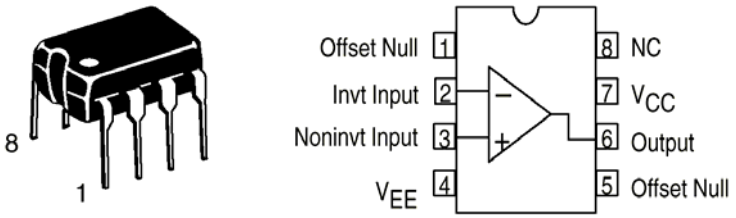
$$v_{i2} = 0 \quad v_o = \left(A_{dm} + \frac{A_{cm}}{2} \right) v_{i1} = A_1 v_{i1} \quad \text{(negative)} \qquad \text{(11A.12a)}$$

$$v_{i1} = 0 \quad v_o = \left(-A_{dm} + \frac{A_{cm}}{2} \right) v_{i2} = A_2 v_{i2} \quad \text{(positive)} \qquad \text{(11A.14b)}$$

Therefore, we generally call the inputs:

- 1 = inverting input (–)
- 2 = non inverting input (+)

Typical 8-pin package details are shown below:



TL071 package details

Figure 11A.8

References

Sedra, A. and Smith, K.: *Microelectronic Circuits*, Saunders College Publishing, New York, 1991.