# Lecture 12A – Op-Amp Circuits

*An op-amp model. The ideal op-amp. The inverting amplifier. The noninverting amplifier. The voltage follower. An adder circuit. Integrator circuits. A precision half wave rectifier.*

## An Op-Amp Model

A model of an op-amp is shown below:

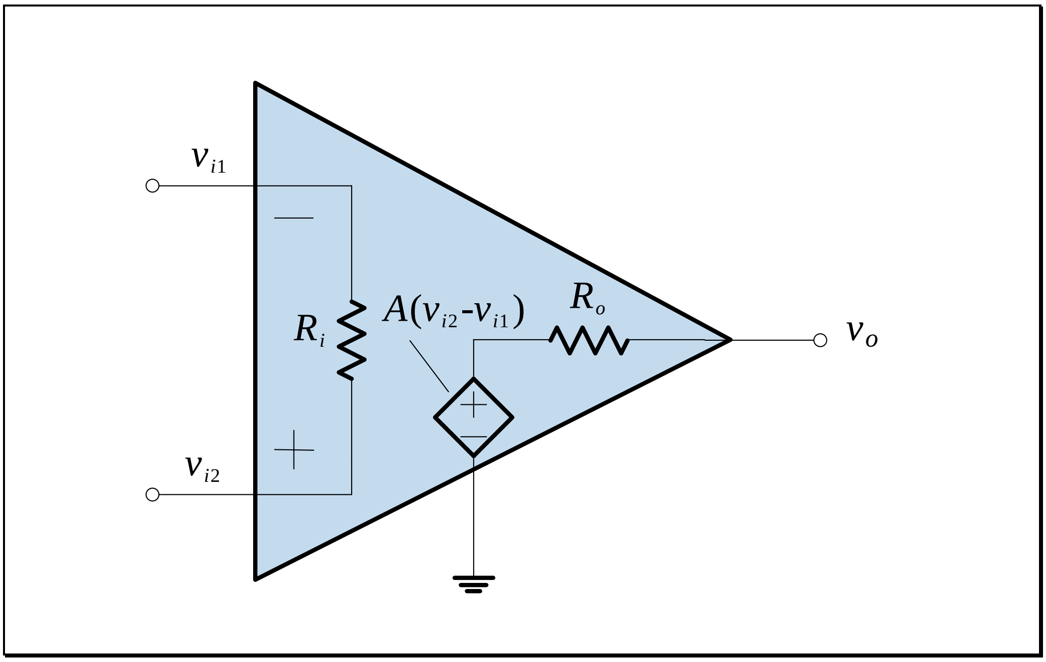


**Figure 12A.1**

Typical values for the op-amp model elements are as follows:

$$R_i = 1\,\text{M}\Omega, \quad R_o = 75\,\Omega, \quad A = 2\times 10^5 \tag{12A.1}$$

To analyze the circuit, we will make three assumptions:

- Since $R_i$ is very large, we will assume it to be infinite.
- Since $R_o$ is very small, we will assume it be zero.
- Since $A$ is very large, we will assume it to be infinite.

These assumptions lead to the model for an ideal o-amp.

## The Ideal Op-Amp

An ideal op-amp has the following parameter values:

The ideal op-amp's parameters

$$\begin{aligned} A &= \infty \\ R_i &= \infty \\ R_o &= 0 \end{aligned} \tag{12A.2}$$

If there is a *negative* feedback path (i.e. a connection between the output of the amplifier and the inverting input terminal), then the op-amp will have a finite output voltage. It follows that:

$$\begin{aligned} v_o &= A(v_{i2} - v_{i1}) \\ v_{i2} - v_{i1} &= \frac{v_o}{A} = \frac{v_o}{\infty} = 0 \end{aligned} \tag{12A.3}$$

Therefore:

The *virtual* short circuit is the key to analysing op-amp circuits

$$\boxed{v_{i1} = v_{i2}} \tag{12A.4}$$

The input to the op-amp looks like a short circuit for voltages, but due to the input resistance being infinite, it looks like an open circuit for currents. The input terminals can therefore be considered a *virtual short circuit*. We will use the virtual short circuit concept frequently.

## The Inverting Amplifier

The inverting amplifier circuit is shown below:

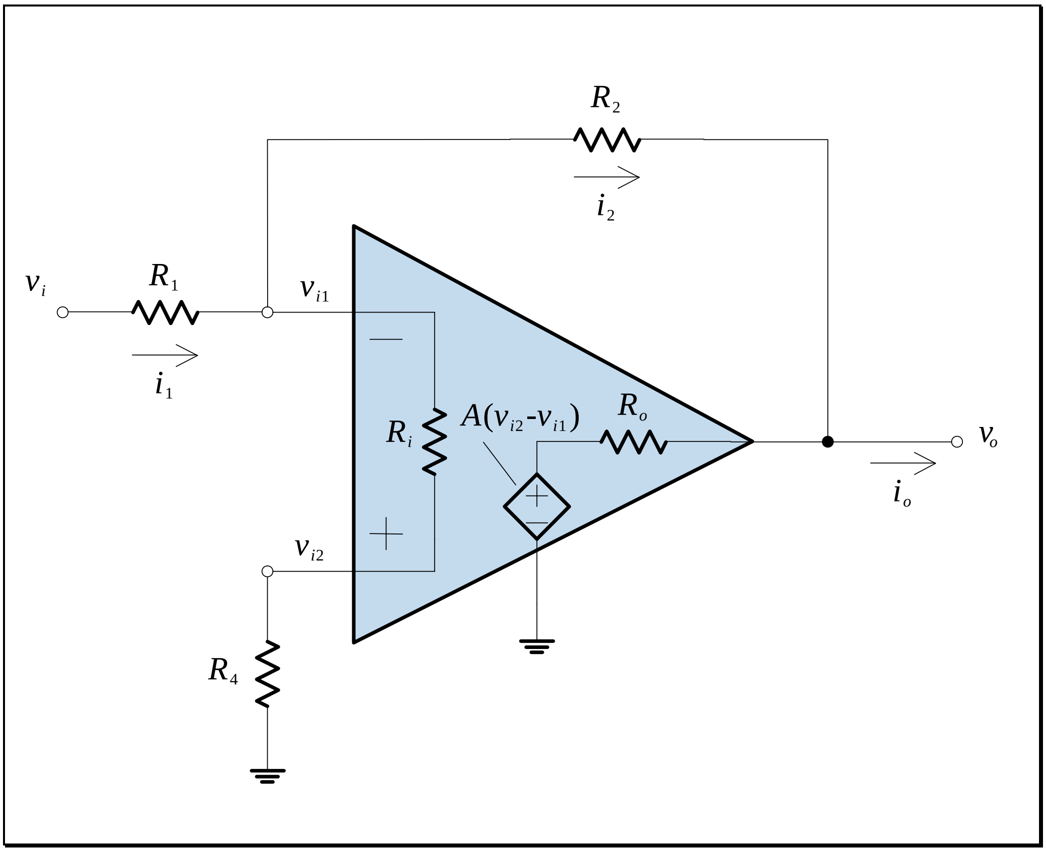


**Figure 12A.2**

It is called inverting because the output will be inverted (which implies a negative gain).

The virtual short circuit concept is very important because it allows us to analyze a circuit very quickly. To see this, we will analyze the circuit using the ideal op-amp model and the concept of a virtual short circuit, and then see how things change with a finite value of *A*.

With a virtual short circuit, the inverting amplifier becomes:

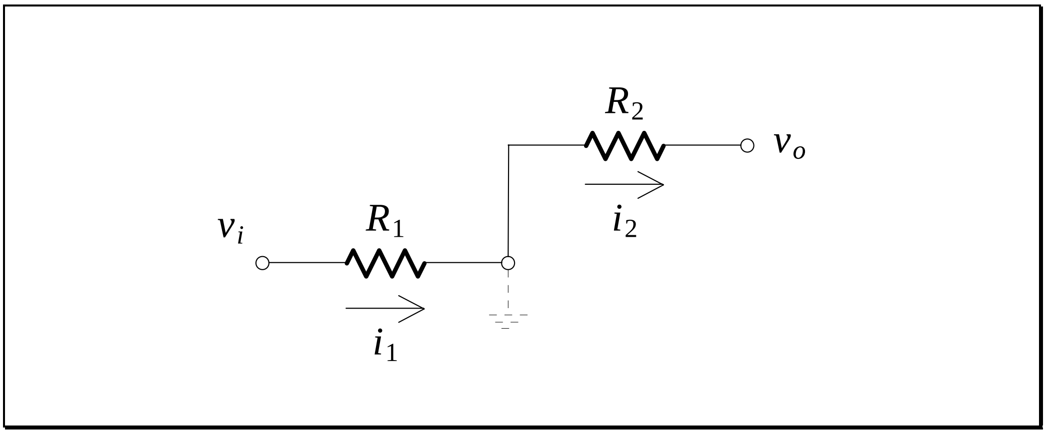


**Figure 12A.3**

**Gain**

There is only one current, so:

$$i_1 = \frac{v_i}{R_1} = -\frac{v_o}{R_2} \tag{12A.5}$$

The voltage gain is then:

$$A_v = \frac{v_o}{v_i} = -\frac{R_2}{R_1} \tag{12A.6}$$

**Input Resistance**

With a virtual short circuit, the input resistance is obtained by inspection:

$$R_{\text{in}} = \frac{v_i}{i_1} = R_1 \tag{12A.7}$$

**Output Resistance**

With a virtual short circuit as in Figure 12A.3, the output voltage is independent of any load resistor. Thus, the output resistance of the amplifier is:

$$R_{\text{out}} = 0 \tag{12A.8}$$

**Effect of Finite Open-Loop Gain**

Firstly, we seek a representation of the circuit which corresponds to the Thévenin equivalent:

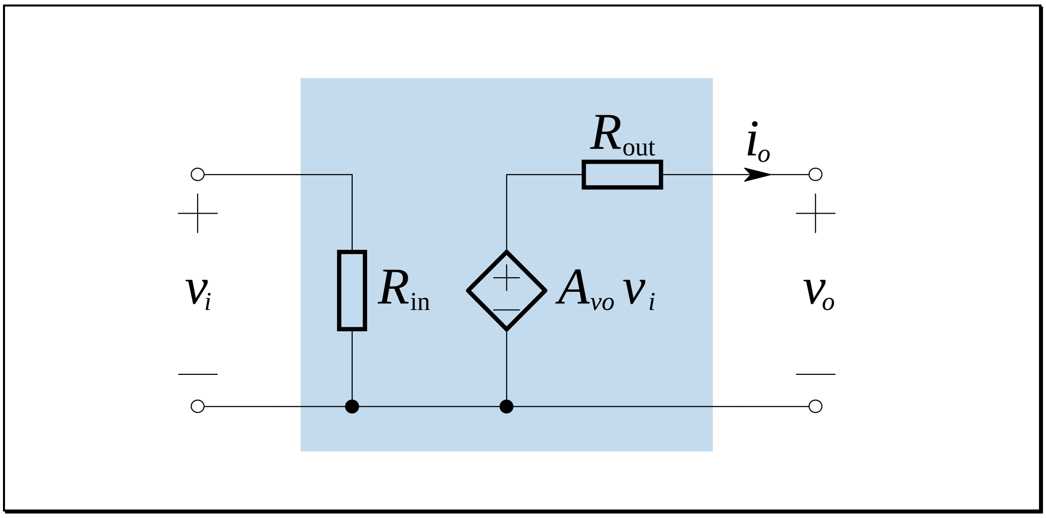


**Figure 12A.4**

With an assumed output current as shown in the figure (the load is not shown), we can write KVL and get:

$$v_o = A_{vo} v_i - R_{\text{out}} i_o \tag{12A.9}$$

We now seek an expression for the output of the real circuit that is in a similar form so that we can identify the open-circuit voltage gain and output resistance by inspection.

To include the effect of a finite *A*, we first introduce the *feedback factor*:

$$\beta = \frac{R_1}{R_1 + R_2} \tag{12A.10}$$

Note that:

$$1 - \beta = \frac{R_2}{R_1 + R_2} \tag{12A.11}$$

which is an expression that will be used later.

# 12A.6

With reference to Figure 12A.2, we now perform KCL at the input:

$$\frac{v_{i1}-v_i}{R_1}+\frac{v_{i1}-v_o}{R_2}=0 \tag{12A.12}$$

Multiplying through by $R_1R_2$ and rearranging, we get:

$$\begin{aligned} v_{i1} &= \frac{R_2}{R_1+R_2}v_i+\frac{R_1}{R_1+R_2}v_o \\ &= (1-\beta)v_i+\beta v_o \end{aligned} \tag{12A.13}$$

KCL at the output gives:

$$\frac{v_o-v_i}{R_1+R_2}+\frac{v_o-(-Av_{i1})}{R_o}+i_o=0 \tag{12A.14}$$

Substituting the expression for $v_{i1}$ from Eq. (12A.13) we get:

$$\frac{v_o-v_i}{R_1+R_2}+\frac{v_o+A(1-\beta)v_i+A\beta v_o}{R_o}+i_o=0 \tag{12A.15}$$

Rearranging we get:

$$v_o\left(\frac{1}{R_1+R_2}+\frac{1+A\beta}{R_o}\right)=\left(\frac{1}{R_1+R_2}-\frac{A(1-\beta)}{R_o}\right)v_i-i_o \tag{12A.16}$$

If we now let:

$$\frac{1}{R_{\text{out}}}=\frac{1}{R_1+R_2}+\frac{(1+A\beta)}{R_0} \tag{12A.17}$$

then we can see that the output resistance is composed of two resistances in parallel:

$$R_{\text{out}} = (R_1 + R_2) \,||\, [R_0 / (1 + A\beta)] \tag{12A.18}$$

This is usually a very small resistance. As an example, an inverting amplifier with a nominal gain of $-R_2/R_1 = -10$ ($\beta = 1/11$) designed using an op-amp with $R_o = 100\,\Omega$ and $A = 10^5$ will have $R_{\text{out}} \approx 11\,\text{m}\Omega$.

We can now rewrite Eq. (12A.16) using our new definition of $R_{\text{out}}$:

$$v_o = \left( \frac{1}{R_1 + R_2} - \frac{A(1-\beta)}{R_o} \right) R_{\text{out}} v_i - R_{\text{out}} i_o \tag{12A.19}$$

This is similar to Eq. (12A.9). By comparison, we can easily identify the open-circuit voltage gain:

$$\begin{aligned}
A_{vo} &= \left( \frac{1}{R_1 + R_2} - \frac{A(1-\beta)}{R_o} \right) R_{\text{out}} \\
&= \left( \frac{R_o - A(1-\beta)(R_1 + R_2)}{(R_1 + R_2) R_o} \right) \frac{(R_1 + R_2) R_o / (1 + A\beta)}{R_1 + R_2 + R_o / (1 + A\beta)} \\
&= \frac{R_o - A(1-\beta)(R_1 + R_2)}{(R_1 + R_2)(1 + A\beta) + R_o} \\
&= \frac{R_o - AR_2}{R_1 + R_2 + AR_1 + R_o} \\
&= \frac{-R_2 + R_o / A}{R_1 + (R_1 + R_2 + R_o)/A}
\end{aligned} \tag{12A.20}$$

With large open-loop gain *A*, the gain expression reduces to $A_v = -R_2/R_1$.

To obtain the input resistance, we do KCL at the inverting terminal:

$$i_1 = \frac{v_{i1} - v_o}{R_2} = \frac{v_{i1} - A(0 - v_{i1})}{R_2} = \frac{v_{i1}(1 + A)}{R_2}$$

$$\frac{v_{i1}}{i_1} = \frac{R_2}{1 + A} \tag{12A.21}$$

and so:

$$R_{\text{in}} = R_1 + \frac{R_2}{1 + A} \tag{12A.22}$$

With large open-loop gain *A*, the input resistance reduces to $R_{\text{in}} = R_1$.

**Resistor $R_4$**

Why do we need to put resistor $R_4$ on the noninverting terminal of the op-amp, if it is at common potential and carries no current?

The standard input stage of integrated circuit op-amps is a DC coupled differential amplifier. As there are no input coupling capacitors, a proportion of the DC bias currents circulate in the input and feedback circuits. To find the DC output voltage of the closed-loop amplifier due to the input bias current, we set the signal source to zero and obtain the circuit below:

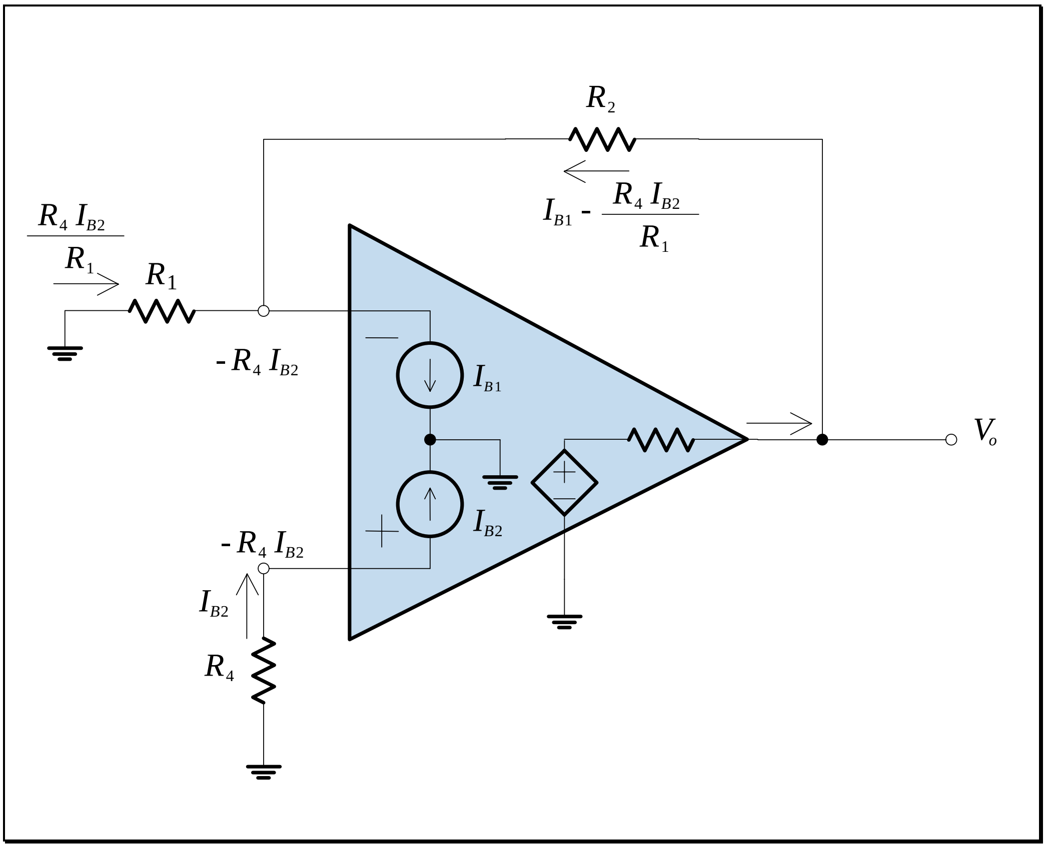


**Figure 12A.5**

With $R_4 = 0$, the output DC voltage is given by:

$$V_o = R_2 I_{B1} \tag{12A.23}$$

which can be significant if $R_2$ is large.

With $R_4 \neq 0$, the output DC voltage is given by:

$$V_o = -R_4 I_{B2} + R_2\left(I_{B1} - R_4/R_1\, I_{B2}\right) \tag{12A.24}$$

For the case $I_{B1} = I_{B2} = I_B$, we get:

$$V_o = \left[R_2 - R_4\left(1 + R_2/R_1\right)\right]I_B \tag{12A.25}$$

We may reduce $V_o$ by selecting $R_4$ such that:

$$R_4 = \frac{R_2}{1 + R_2/R_1} = \frac{R_2 R_1}{R_1 + R_2} = R_1 \parallel R_2 \tag{12A.26}$$

Therefore, to reduce the effect of DC bias currents, we should select $R_4$ to be equal to the parallel equivalent of $R_1$ and $R_2$. Having selected this value, substitution into Eq. (12A.24) gives:

$$V_o = R_2\left(I_{B1} - I_{B2}\right) \tag{12A.27}$$

If we define the *input offset current* as the difference between the two input bias currents:

$$I_{\text{off}} = I_{B1} - I_{B2} \tag{12A.28}$$

then:

$$V_o = R_2 I_{\text{off}} \tag{12A.29}$$

which is usually about an order of magnitude smaller than the value obtained without $R_4$.

## The Noninverting Amplifier

The noninverting circuit has the input signal connected to the noninverting terminal of the op-amp in some way:

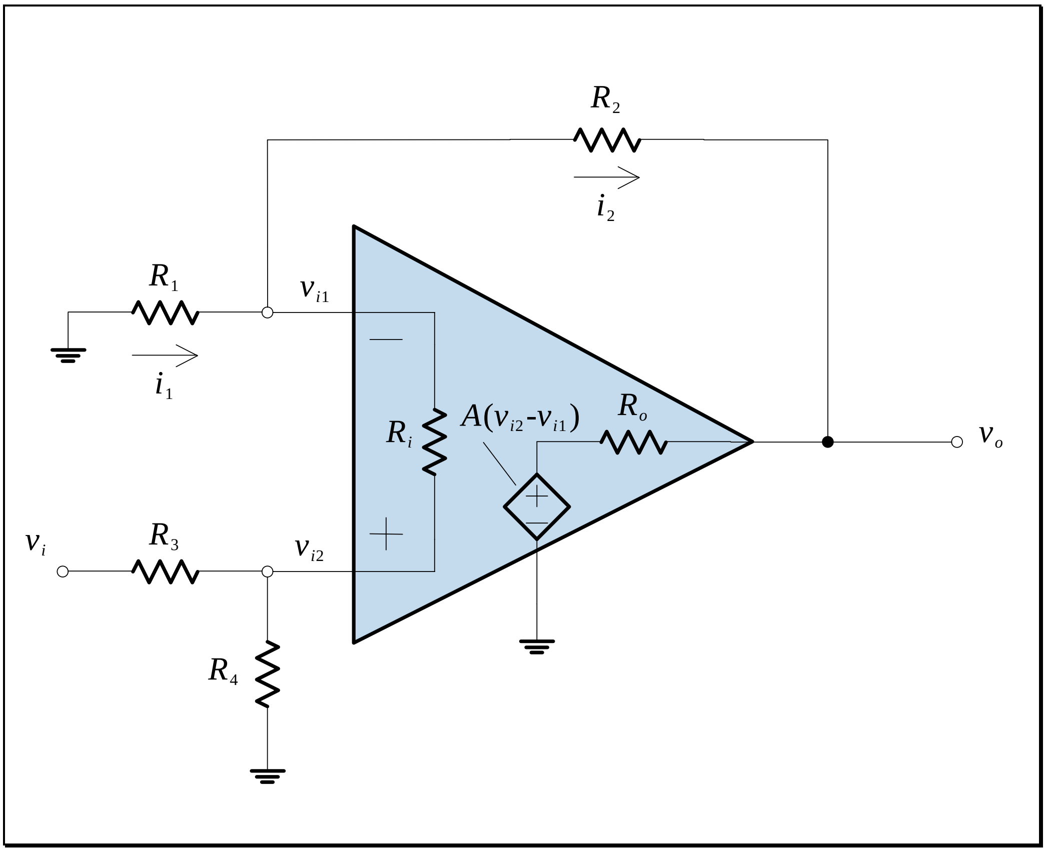


**Figure 12A.6**

An analysis of this circuit follows. First the gain:

$$v_{i2} \approx v_{i1}$$

$$\frac{R_4}{R_3 + R_4} v_i \approx \frac{R_1}{R_1 + R_2} v_o$$

$$\frac{v_o}{v_i} \approx \frac{1 + R_2/R_1}{1 + R_3/R_4} \tag{12A.30}$$

The input and output resistance are obtained in the same way as before:

$$R_{\text{in}} \approx R_3 + R_4 \tag{12A.31a}$$

$$R_{\text{out}} \approx 0 \tag{12A.26b}$$

## The Voltage Follower

The voltage follower is used instead of the source or emitter follower where precision is required. It is used for impedance matching.

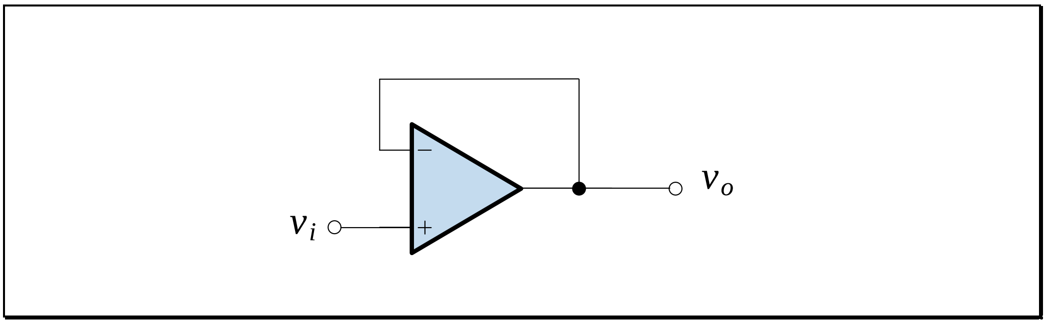


**Figure 12A.7**

To analyze the circuit we note that:

$$R_2 = R_3 = 0 \quad R_1 = R_4 = \infty \tag{12A.32a}$$

$$\therefore A_v \approx 1 \quad R_{\text{in}} \approx \infty \quad R_{\text{out}} \approx 0 \tag{12A.27b}$$

The voltage follower is used to provide isolation between two parts of a circuit when it is required to join them without interaction. For example, to couple a high resistance source to a low resistance load, without suffering a voltage drop, we insert a buffer between source and load:

A buffer is used to couple a high impedance to a low impedance

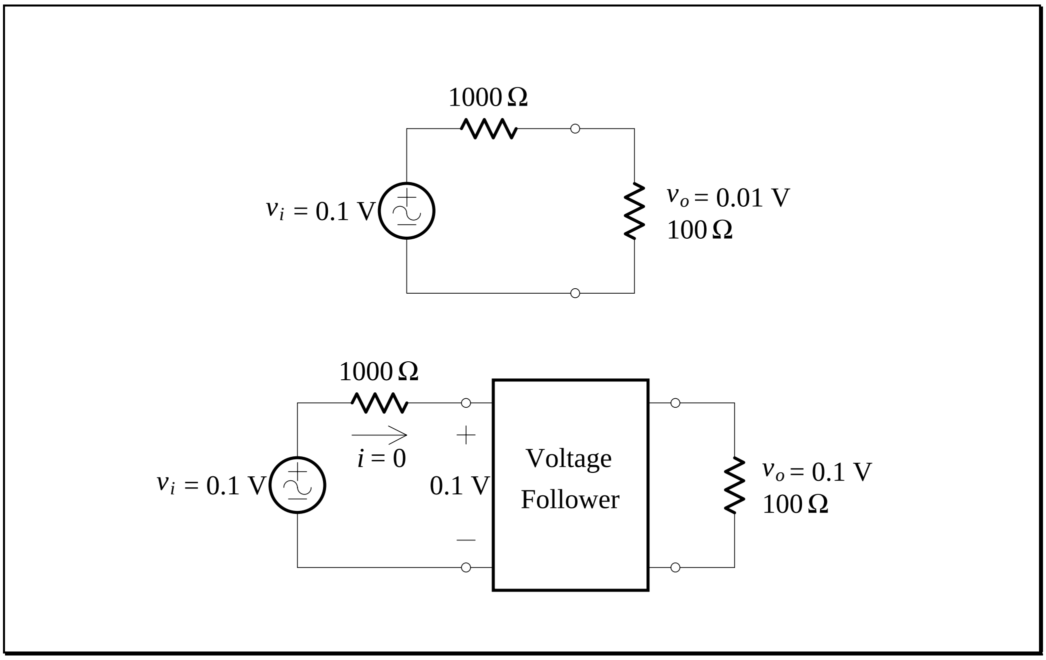


**Figure 12A.8**

## An Adder Circuit

An adder circuit performs the mathematical operation of addition on two (or more) voltages (hence the name operational amplifier):

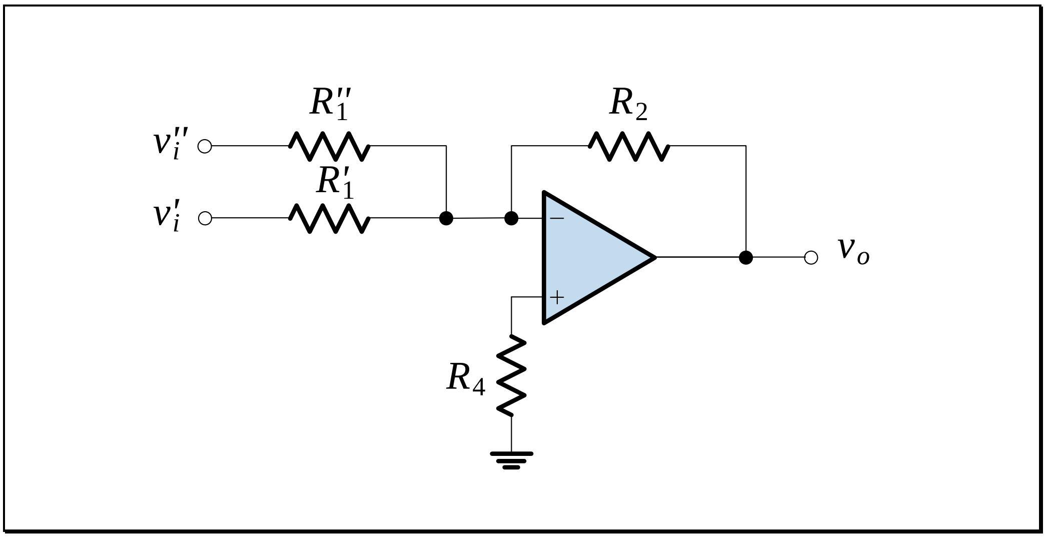


**Figure 12A.9**

We can use superposition, and the concept of the virtual short circuit, to obtain the gain of this circuit:

$$v_o = -R_2\left(\frac{v_i'}{R_1'} + \frac{v_i''}{R_1''}\right) \tag{12A.33}$$

## Integrator Circuits

The ideal integrator circuit is:

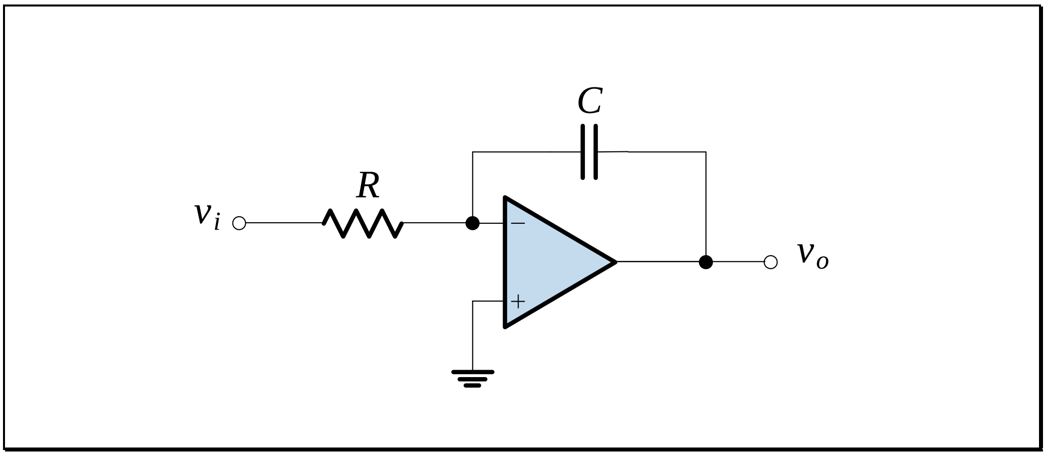


**Figure 12A.10**

We use the virtual short circuit concept to analyze the gain (it is essentially the same analysis as for the inverting amplifier). KCL at the inverting terminal gives:

$$\frac{v_i}{R} = -C\frac{dv_o}{dt}$$

$$v_o = -\frac{1}{RC}\int_0^t v_i dt + v_o(0) \tag{12A.34}$$

Unfortunately, this circuit suffers from the fact that any DC at the input, such as the inherent input offset voltages and currents of the op-amp, will be integrated and eventually cause the output of the op-amp to saturate.

A practical circuit that alleviates this problem is known as the Miller integrator, shown below:

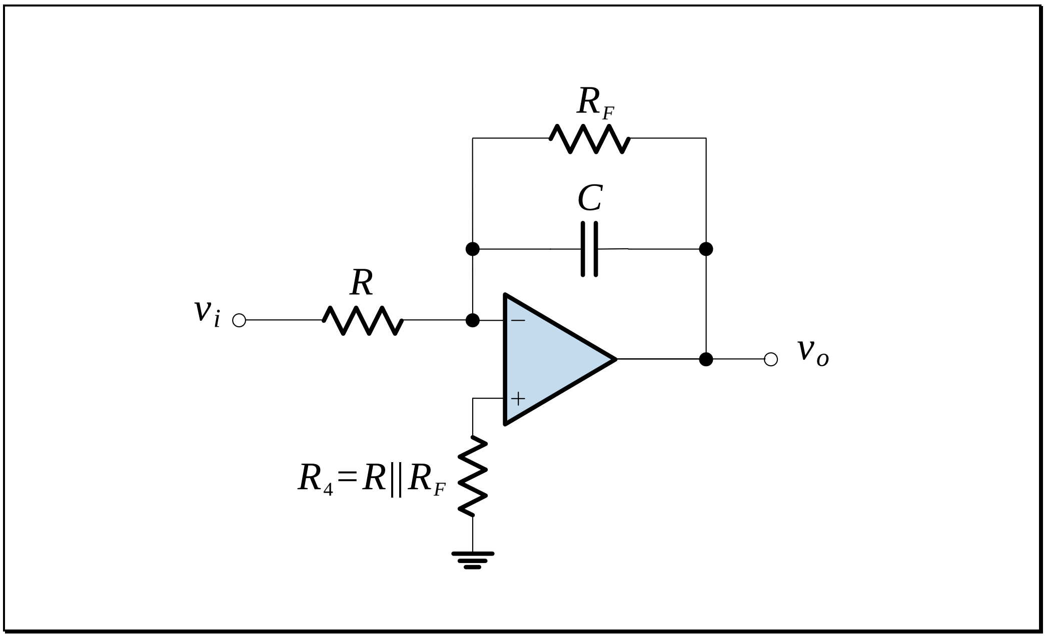


**Figure 12A.11**

The Miller integrator provides a path for the DC offset currents $V_{OS}/R$ and $I_{OS}$, with the result that the output has a DC component given by:

$$V_o = (1 + R_F/R)V_{OS} + R_F I_{OS} \tag{12A.35}$$

To keep the DC offset at the output of the integrator low, we should select a small $R_F$. Unfortunately, however, the lower the value of $R_F$, the less ideal the integrator becomes. Thus selecting a value for $R_F$ is a trade-off between DC performance and integrator performance.

## A Precision Half Wave Rectifier

A precision half wave rectifier gets around the problem of the forward bias voltage drop with real diodes. We can rectify signals less than 0.7 V with this circuit:

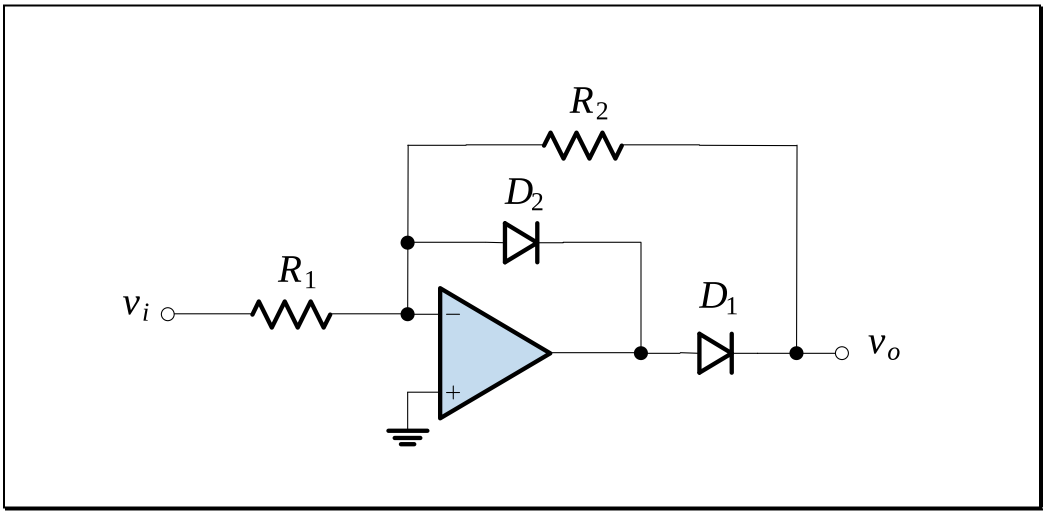


**Figure 12A.12**

To analyze this circuit, we firstly remember that the diode is a nonlinear element so that linear circuit analysis does not apply. We assume that somehow the op-amp is working so that there is a virtual short circuit at its input.

In the positive half cycle, with the op-amp working, the current is to the right in resistor $R_1$. The current cannot enter the op-amp inverting terminal, due to the infinite input resistance of the op-amp, so it must go up. Diode D2 is in the right direction to conduct this current, so it will. Since the diode is conducting, the voltage at the output terminal of the op-amp will be about -0.7 V. With D1 assumed off, the voltage across it is -0.7 V so our assumption is correct. The resistor $R_2$ does not conduct any current, so the voltage drop across it is also zero. The output of the circuit is therefore 0 V for a positive half cycle.

In the negative half cycle, with the op-amp working, the current is to the left in resistor $R_1$. The current cannot be coming from the op-amp inverting terminal, because it is like an open circuit, so it must be coming from the feedback circuit. Diode D1 is in the right direction to conduct this current, so it will, Since the diode is conducting, the voltage at the output of the circuit will be:

$$v_o = -\frac{R_2}{R_1} v_i \tag{12A.36}$$

This is determined solely by the external resistors. The voltage at the output terminal of the op-amp will be whatever it has to be to supply this current through D1. For example, it may be 0.7 V above the output voltage for large input signals, or it may be 0.5 V above the output voltage for small input signals.

The voltage across D2 is such as to reverse bias it. The purpose of D2 is to let the op-amp create a virtual short circuit for the positive half cycle. Otherwise the op-amp would saturate, and the output would not be zero.

## References

Sedra, A. and Smith, K.: *Microelectronic Circuits*, Saunders College Publishing, New York, 1991.